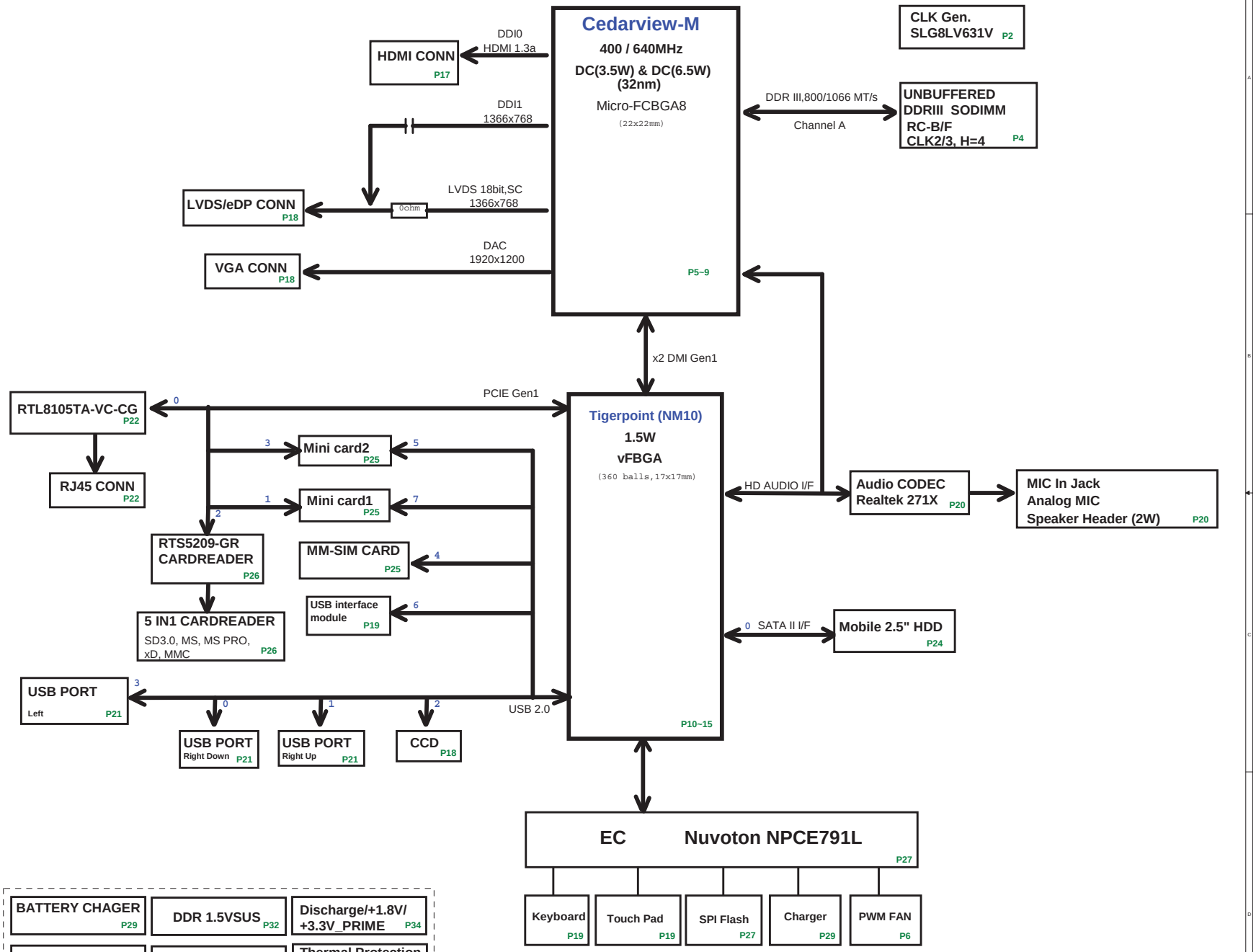
ZE7 Block Diagram (Intel Cedar Trail-M Platform)



Quanta Computer Inc.

PROJECT : ZE7

Size	Document Number	Rev
	Block Diagram	C3C

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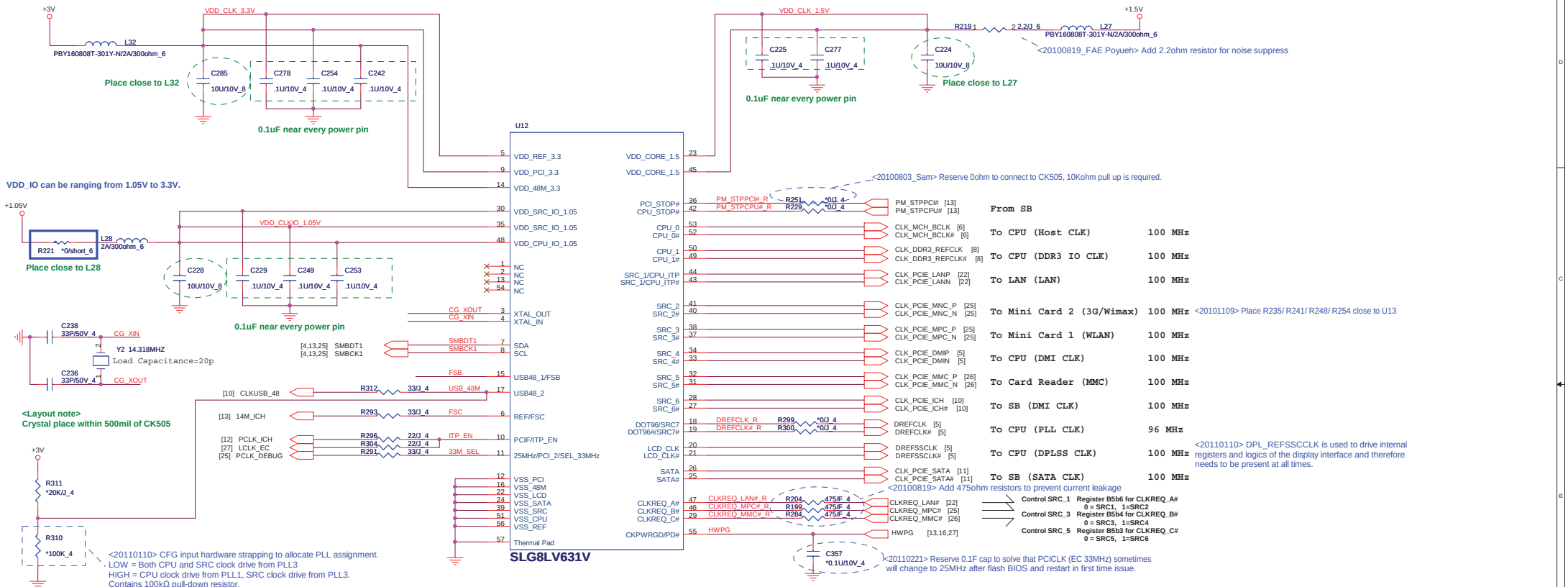
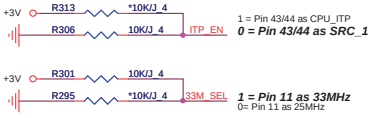
CLK GEN (CLK)

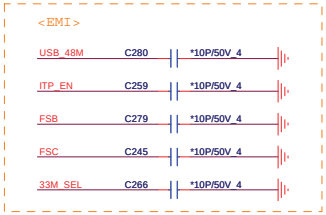
02

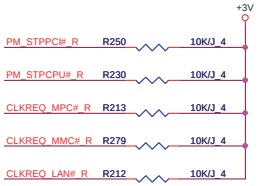




FSC	FSB	Frequency
0	0	133MHz
0	1	166MHz
1	1	200MHz
1	0	100MHz

<20100720_Sam> Keep 100MHz as default.





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	CLOCK GENERATOR	C3C

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	Reserved	C3C
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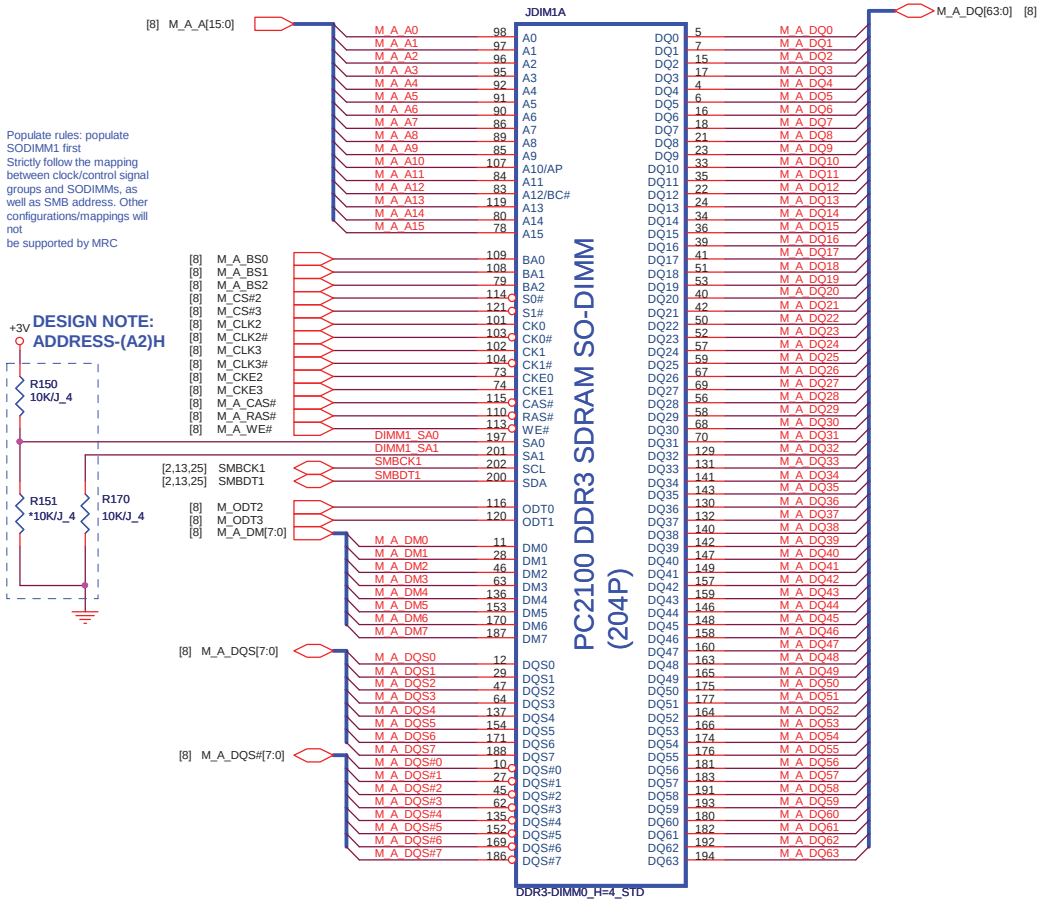
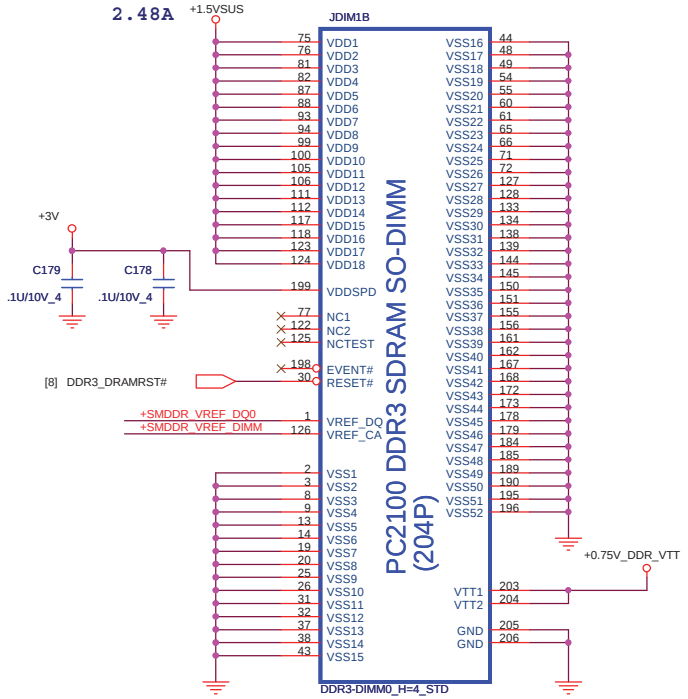
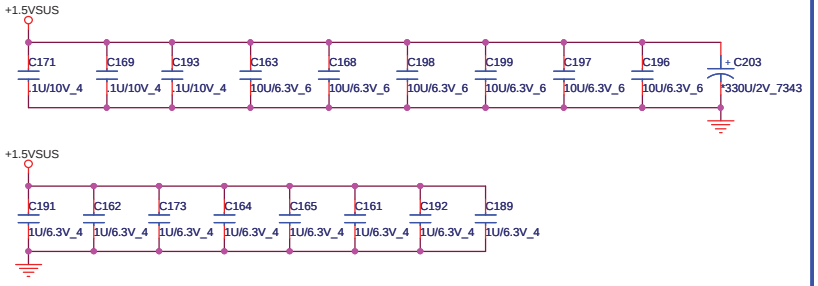
DDR_STD(DDR)

DIMM0 H=4mm

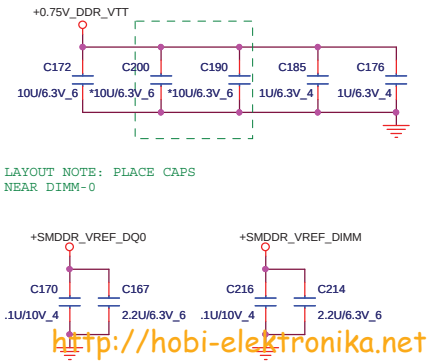




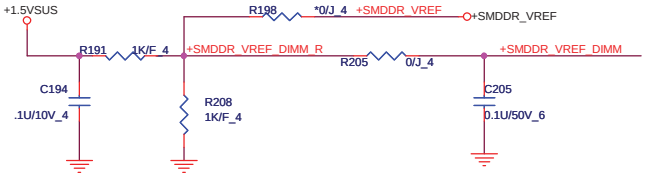
Place these Caps near DIMM0



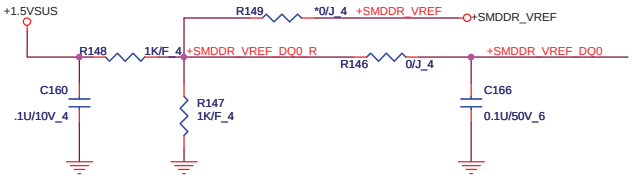
<20100827> Add by DG request

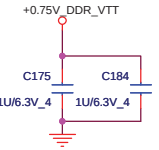


<Layout note>
PLACE TWO 1K RESISTORS CLOSE TO CPU DIMM ON DDR_VREF_CA



<Layout note>
PLACE TWO 1K RESISTORS CLOSE TO CPU DIMM ON DDR_VREF_DQ





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Size	Document Number	Rev
	DDRIII SO-DIMM-0	C3C
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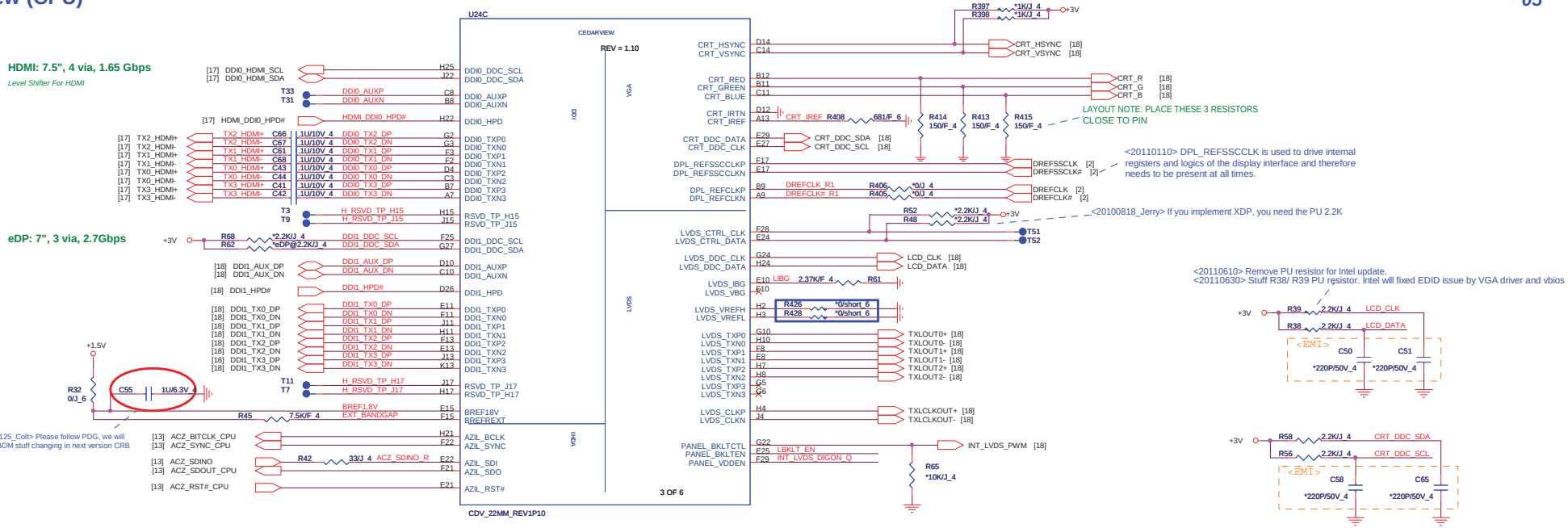
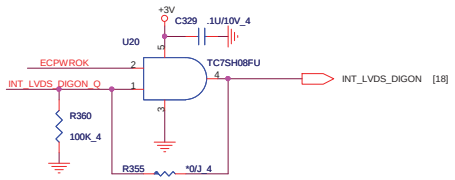
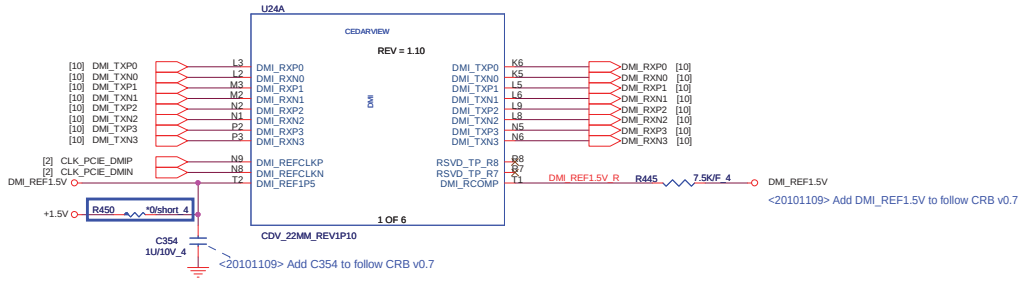
Cedar View (CPU)

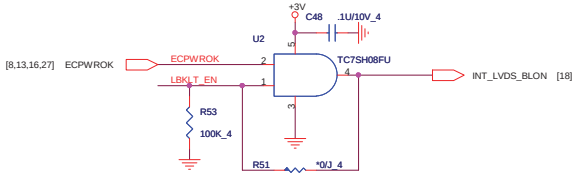


LCD Panel Power (LDS)





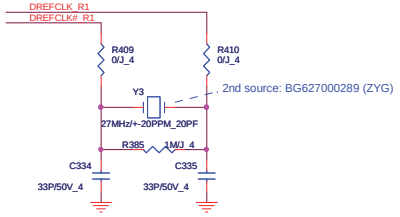
LCD Panel Backlight (LDS)



For HDMI deep color mode support (HDM)

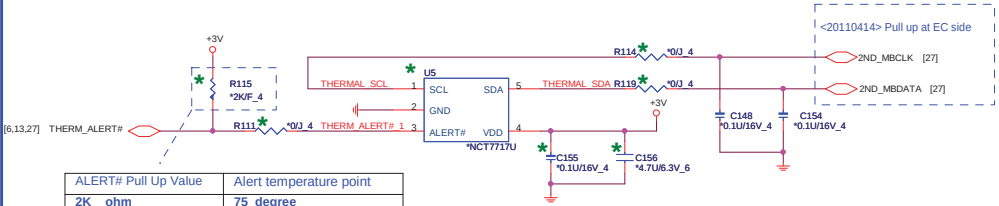
<20100727_Sam> Customer must to use 27MHz due to accuracy concerns(<1000ppm) from Intel silicon perspective.

LAYOUT NOTE: PLACE CLOSE TO PIN



THERMAL SENSOR (THM)

<20110414> Unstuff Thermal Sensor and related circuit.



ALERT# Pull Up Value	Alert temperature point
2K ohm	**75 degree**
7.5K ohm	90 degree
10.5K ohm	100 degree
14K ohm	105 degree
18.7K ohm	110 degree

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	Cedarview DMI/Display	C3C
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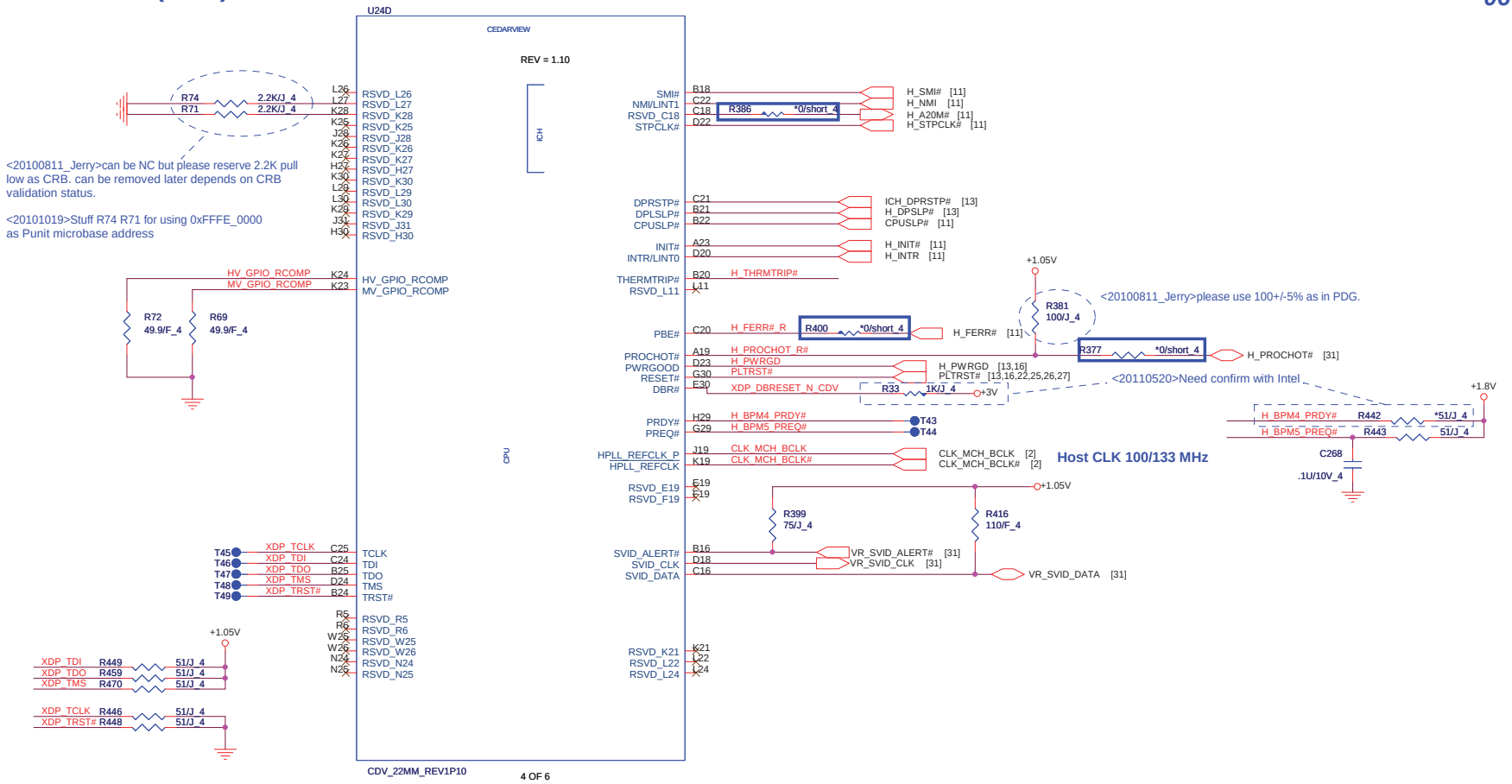
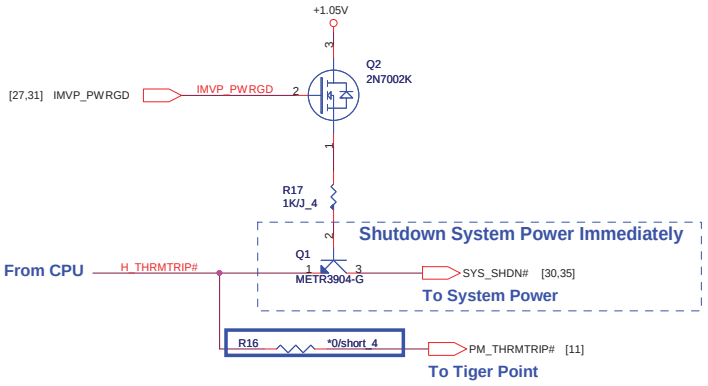
Cedar View (CPU)

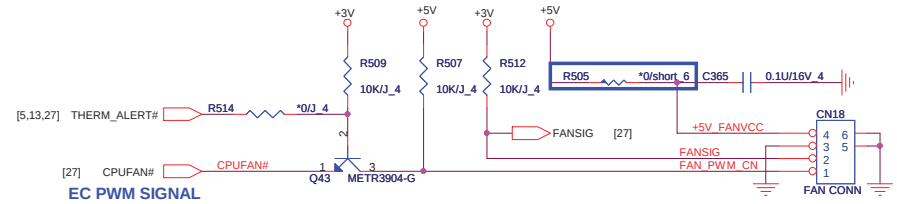
06

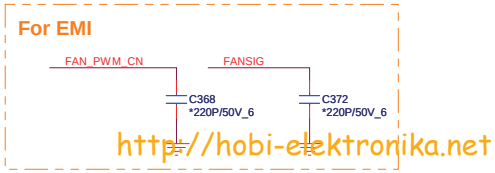


125 Degree Protection(CPU)



CPU FAN CTRL(THM)





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	Cedarview Miscellaneous	C3C
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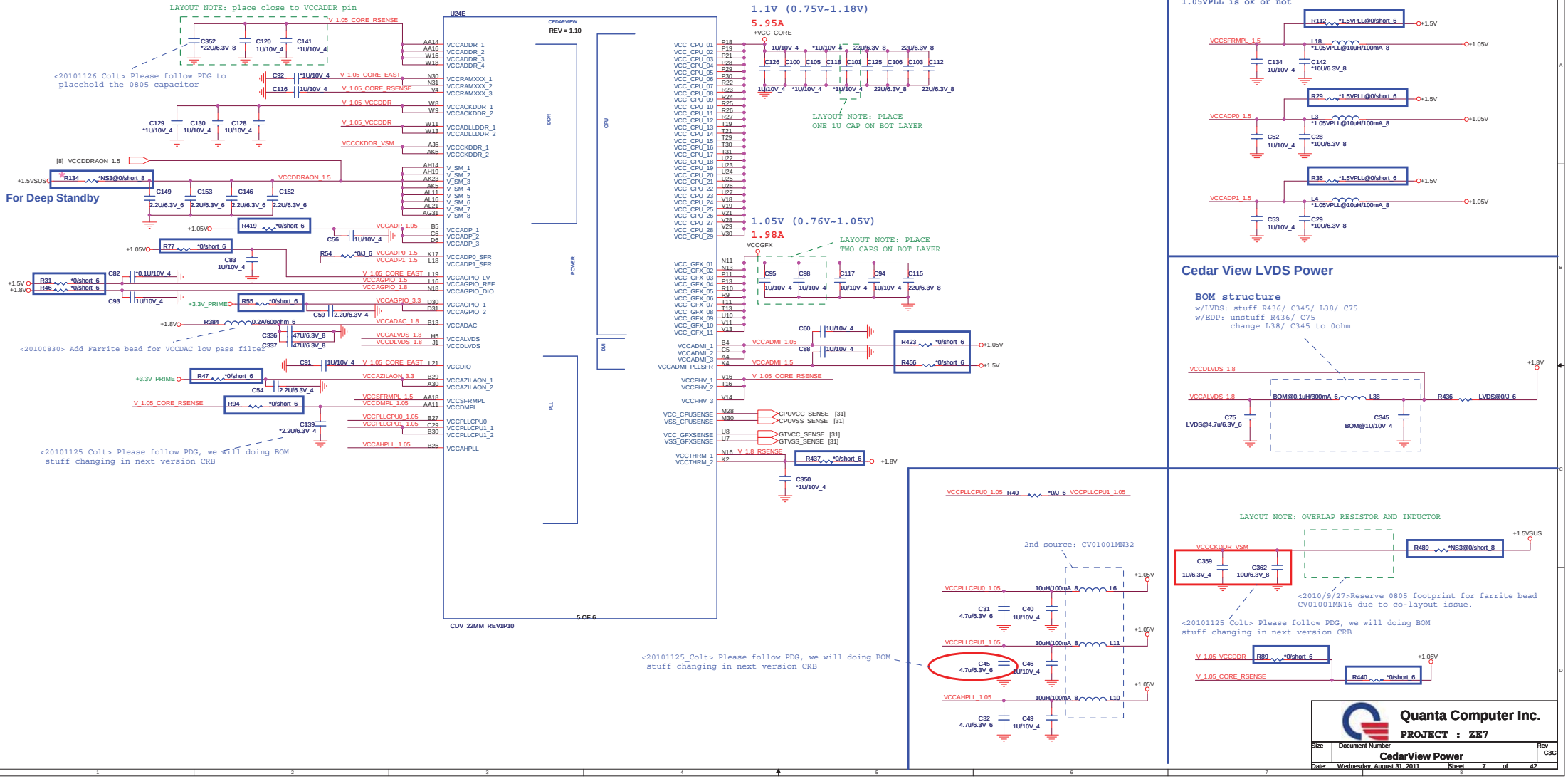
Cedar View (CPU)



Cedar View PLL Power

07

Default stuff 1.5VPLL, Intel verify whether 1.05VPLL is ok or not

Cedar View LVDS Power

BOM structure

w/LVDS: stuff R436/ C345/ L38/ C75
w/EDP: unstuff R436/ C75
change L38/ C345 to 0ohm

LAYOUT NOTE: OVERLAP RESISTOR AND INDUCTOR

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Cedar View (CPU)

U24B

CEDARVIEW

REV = 1.10

[4] M_A_A[15:0]

M_A_A0 AK14 DDR3_MA0
M_A_A1 AK16 DDR3_MA1
M_A_A2 AJ14 DDR3_MA2
M_A_A3 AJ16 DDR3_MA3
M_A_A4 AK18 DDR3_MA4
M_A_A5 AH18 DDR3_MA5
M_A_A6 AJ18 DDR3_MA6
M_A_A7 AK20 DDR3_MA7
M_A_A8 AJ20 DDR3_MA8
M_A_A9 AH20 DDR3_MA9
M_A_A10 AJ12 DDR3_MA10
M_A_A11 AK21 DDR3_MA11
M_A_A12 AJ21 DDR3_MA12
M_A_A13 AJ8 DDR3_MA13
M_A_A14 AH22 DDR3_MA14
M_A_A15 AJ22 DDR3_MA15

[4] M_A_WE# → M_A_WE# AH10 DDR3_WE#
[4] M_A_CAS# → M_A_CAS# AJ10 DDR3_CAS#
[4] M_A_RAS# → M_A_RAS# AJ11 DDR3_RAS#

[4] M_A_BS0 → M_A_BS0 AK12 DDR3_BS0
[4] M_A_BS1 → M_A_BS1 AH13 DDR3_BS1
[4] M_A_BS2 → M_A_BS2 AK22 DDR3_BS2

AH12 DDR3_CS#0
AH8 DDR3_CS#1
[4] M_CS#2 → M_CS#2 AK11 DDR3_CS#2
[4] M_CS#3 → M_CS#3 AK8 DDR3_CS#3

AH23 DDR3_CKE0
AJ24 DDR3_CKE1
[4] M_CKE2 → M_CKE2 AK24 DDR3_CKE2
[4] M_CKE3 → M_CKE3 AH24 DDR3_CKE3

AK10 DDR3_ODT0
AK7 DDR3_ODT1
[4] M_ODT2 → M_ODT2 AL9 DDR3_ODT2
[4] M_ODT3 → M_ODT3 AJ7 DDR3_ODT3

AG15 DDR3_CK0
AF15 DDR3_CK#0
AF17 DDR3_CK1
AG17 DDR3_CK#1
[4] M_CLK2 → M_CLK2 AD17 DDR3_CK2
[4] M_CLK2# → M_CLK2# AC17 DDR3_CK#2
[4] M_CLK3 → M_CLK3 AC15 DDR3_CK3
[4] M_CLK3# → M_CLK3# AD15 DDR3_CK#3

DDR3_DRAMRST#_R → AK25 DDR3_DRAMRST#

DDR_VREF → AJ27 DDR3_VREF
AL28 DDR3_VREF_NCTF

[2] CLK_DDR3_REFCLK → AC19 DDR3_REFP
[2] CLK_DDR3_REFCLK# → AB19 DDR3_REFN

DDRAM_PWROK → AA5 DDR3_DRAM_PWROK 1.5V
DELAY_VR_PWRGD_CDV → W7 DDR3_VCCA_PWROK 1.5V

M_ODTPU AJ26 DDR3_ODTPU
M_CMDPU AJ25 DDR3_CMDPU
M_DQPU AK27 DDR3_DQPU

AB11 RSVD_TP_AB11
AB13 RSVD_TP_AB13
AF19 RSVD_TP_AF19
AG19 RSVD_TP_AG19

DDR3

[4] M_A_DM[7:0]

M_A_DM0 Y28 DDR3_DM0
M_A_DM1 AB26 DDR3_DM1
M_A_DM2 AE30 DDR3_DM2
M_A_DM3 AB21 DDR3_DM3
M_A_DM4 AG11 DDR3_DM4
M_A_DM5 AG2 DDR3_DM5
M_A_DM6 AB8 DDR3_DM6
M_A_DM7 AA3 DDR3_DM7

DDR3_DQ0 Y30 M_A_DQ0
DDR3_DQ1 Y29 M_A_DQ1
DDR3_DQ2 AC30 M_A_DQ2
DDR3_DQ3 AC31 M_A_DQ3
DDR3_DQ4 W31 M_A_DQ4
DDR3_DQ5 W28 M_A_DQ5
DDR3_DQ6 AB28 M_A_DQ6
DDR3_DQ7 AB30 M_A_DQ7
DDR3_DQ8 AA24 M_A_DQ8
DDR3_DQ9 AA22 M_A_DQ9
DDR3_DQ10 AE27 M_A_DQ10
DDR3_DQ11 AE26 M_A_DQ11
DDR3_DQ12 AB27 M_A_DQ12
DDR3_DQ13 AA25 M_A_DQ13
DDR3_DQ14 AD25 M_A_DQ14
DDR3_DQ15 AD27 M_A_DQ15
DDR3_DQ16 AD29 M_A_DQ16
DDR3_DQ17 AE29 M_A_DQ17
DDR3_DQ18 AJ30 M_A_DQ18
DDR3_DQ19 AK29 M_A_DQ19
DDR3_DQ20 AD28 M_A_DQ20
DDR3_DQ21 AD30 M_A_DQ21
DDR3_DQ22 AG30 M_A_DQ22
DDR3_DQ23 AJ29 M_A_DQ23
DDR3_DQ24 AE24 M_A_DQ24
DDR3_DQ25 AG24 M_A_DQ25
DDR3_DQ26 AD22 M_A_DQ26
DDR3_DQ27 AC21 M_A_DQ27
DDR3_DQ28 AG27 M_A_DQ28
DDR3_DQ29 AG25 M_A_DQ29
DDR3_DQ30 AG21 M_A_DQ30
DDR3_DQ31 AE21 M_A_DQ31
DDR3_DQ32 AD13 M_A_DQ32
DDR3_DQ33 AD11 M_A_DQ33
DDR3_DQ34 AG8 M_A_DQ34
DDR3_DQ35 AG7 M_A_DQ35
DDR3_DQ36 AG13 M_A_DQ36
DDR3_DQ37 AE13 M_A_DQ37
DDR3_DQ38 AD10 M_A_DQ38
DDR3_DQ39 AF8 M_A_DQ39
DDR3_DQ40 AH2 M_A_DQ40
DDR3_DQ41 AG3 M_A_DQ41
DDR3_DQ42 AD2 M_A_DQ42
DDR3_DQ43 AD3 M_A_DQ43
DDR3_DQ44 AH4 M_A_DQ44
DDR3_DQ45 AK3 M_A_DQ45
DDR3_DQ46 AE2 M_A_DQ46
DDR3_DQ47 AD4 M_A_DQ47
DDR3_DQ48 AD7 M_A_DQ48
DDR3_DQ49 AD6 M_A_DQ49
DDR3_DQ50 AA6 M_A_DQ50
DDR3_DQ51 AB5 M_A_DQ51
DDR3_DQ52 AF8 M_A_DQ52
DDR3_DQ53 AE5 M_A_DQ53
DDR3_DQ54 AB9 M_A_DQ54
DDR3_DQ55 AA8 M_A_DQ55
DDR3_DQ56 AB2 M_A_DQ56
DDR3_DQ57 AB4 M_A_DQ57
DDR3_DQ58 W4 M_A_DQ58
DDR3_DQ59 V3 M_A_DQ59
DDR3_DQ60 AC2 M_A_DQ60
DDR3_DQ61 AB3 M_A_DQ61
DDR3_DQ62 Y2 M_A_DQ62
DDR3_DQ63 W1 M_A_DQ63

DDR3_DQS0 AA30 M_A_DQS0
DDR3_DQS1 AB24 M_A_DQS1
DDR3_DQS2 AE30 M_A_DQS2
DDR3_DQS3 AE22 M_A_DQS3
DDR3_DQS4 AG10 M_A_DQS4
DDR3_DQS5 AF4 M_A_DQS5
DDR3_DQS6 AB6 M_A_DQS6
DDR3_DQS7 Y3 M_A_DQS7

DDR3_DQS#0 AA31 M_A_DQS#0
DDR3_DQS#1 AB25 M_A_DQS#1
DDR3_DQS#2 AF29 M_A_DQS#2
DDR3_DQS#3 AE22 M_A_DQS#3
DDR3_DQS#4 AE10 M_A_DQS#4
DDR3_DQS#5 AE3 M_A_DQS#5
DDR3_DQS#6 AB7 M_A_DQS#6
DDR3_DQS#7 AA2 M_A_DQS#7

M_A_DQ[63:0] [4]
M_A_DQS[7:0] [4]
M_A_DQS#[7:0] [4]

CDV_22MM_REV1P10

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<Layout note>
PLACE RESISTORS AND CAP CLOSE TO CPU DDR_VREF PIN

[7] VCCDDRAON_1.5 — R482 1K/F_4 — +SMDDR_VREF — R492 *0/J_4 — R483 *0/short_4 — R493 1K/F_4 — C360 0.1U/16V_4

<20100810_Jerry> Please refer to Cedar Trail CPET HW section(#454349),
it is to implement Deep Standby. And please waiting the whitepaper for implementation detail.

<20100817_Jerry>DELAY_VR_PWRGOOD on CDV should be connected to the XDP_PWRGOOD because the SV folks expressed a preference on using PWROK over PWRGOOD for CDV. This has changed from PNV to CDV.

T53
[5,13,16,27] ECPWROK — R99 121/F_4 — R98 100/F_4

<20110520>Change 12.1K to 121ohm to follow CRBv1.5
<20110520>Change 10K to 100ohm to follow CRBv1.5

R485 274/F_4 — R488 22.6/F_4 — C361 *0.01U/25V_4 — R484 33.2/F_4

<20100811_Jerry> R485 please follow CRB schematic. (274ohm)

DRAM Reset (CPU)

+1.5VSUS
<20110520>Need to confirm with Intel if we need to add series 100ohm resistor
<20110607>Keep original design first for DRAMRST#
<20110707_Nick> Please un-stuff 1K pull up
R538 *1K/F_4
[4] DDR3_DRAMRST# — R537 *0/short_4 — DDR3_DRAMRST#_NS — R539 *0/short_4 — DDR3_DRAMRST#_R
C159 0.1U/16V_4
<20110607>Keep original design first for DRAMRST#
<20110707_Nick> Please stuff 100K pull down
<20110727> Add C159 to suppress glitch
R474 100K/J_4

<20110727>Connect DDRAM_PWROK between CDV and RT8207L to meet JEDEC timing spec

+1.5VSUS
VCCDDRAON_1.5
R100 10K/J_4
[27,32] DDRAM_PWROK
R97 *0/J_4
C388 *1U/10V_6
<20110727> Reserve C388 for RC delay

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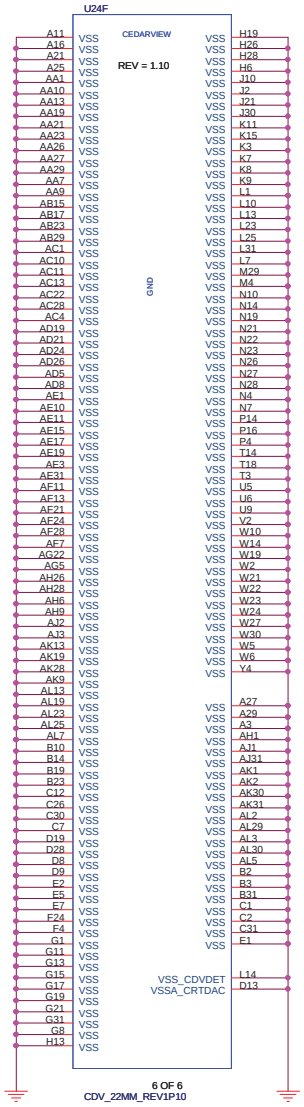
Cedar View (CPU)



Quanta Computer Inc.

PROJECT : ZE7

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	CedarView GND/ Deep Standby	C3C

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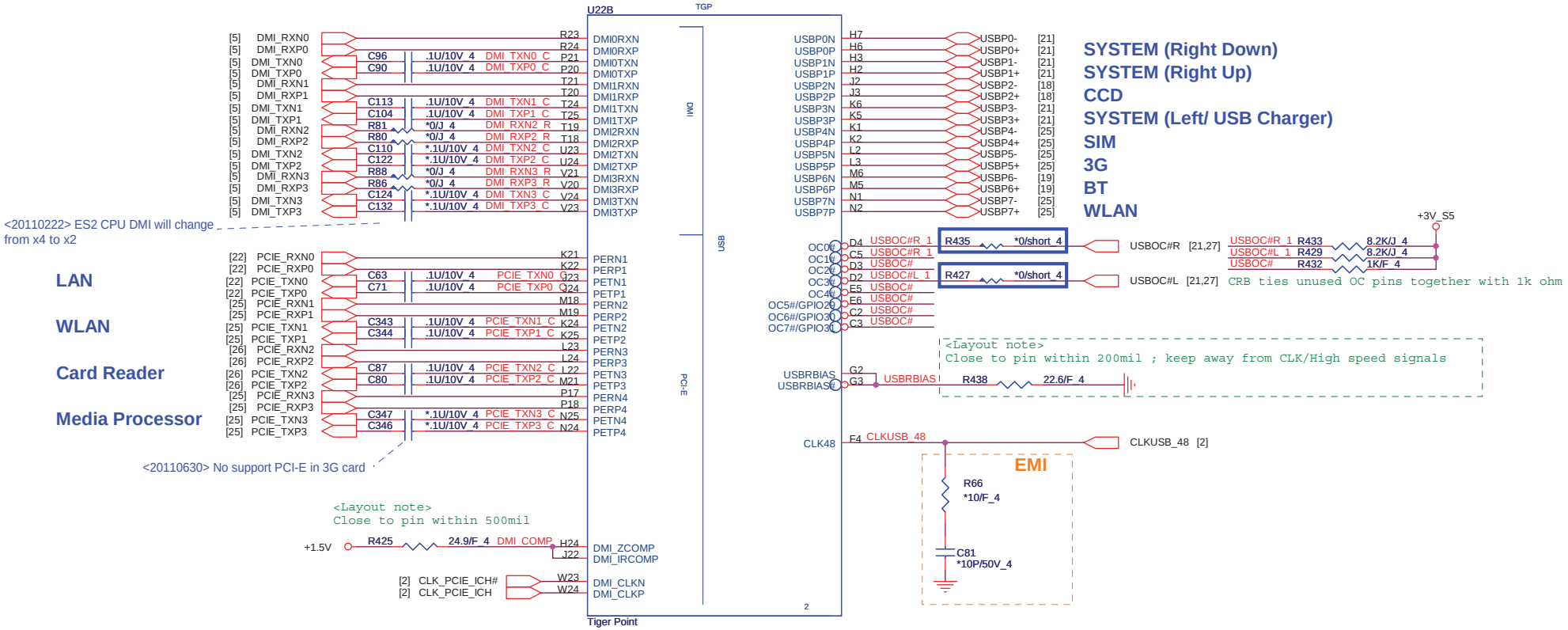
Tiger Point (CLG)



Quanta Computer Inc.		
PROJECT : ZE7		
Size	Document Number: Tiger Point DMI/PCIE/USB	Rev: C3C
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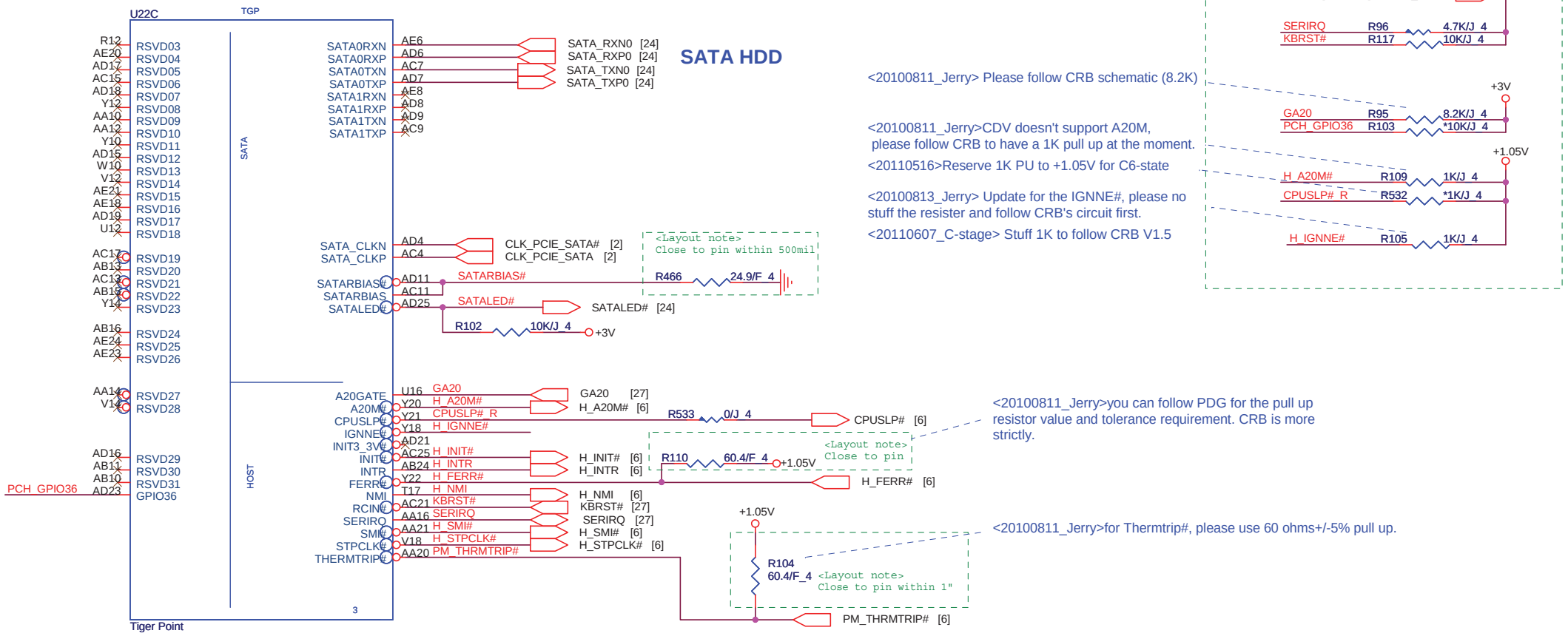
NOTE :
1. CPUSLP# is supported only on nettop platforms.



<20100811_Jerry> Please follow CRB schematic (8.2K)

<20100811_Jerry>CDV doesn't support A20M, please follow CRB to have a 1K pull up at the moment.

<20110516>Reserve 1K PU to +1.05V for C6-state

<20100813_Jerry> Update for the IGNNE#, please no stuff the resister and follow CRB's circuit first.

<20110607_C-stage> Stuff 1K to follow CRB V1.5

<20100811_Jerry>you can follow PDG for the pull up resistor value and tolerance requirement. CRB is more strictly.

<20100811_Jerry>for Thermtrip#, please use 60 ohms+/-5% pull up.

Quanta Computer Inc.
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	Tiger Point Sata/Host	C3C
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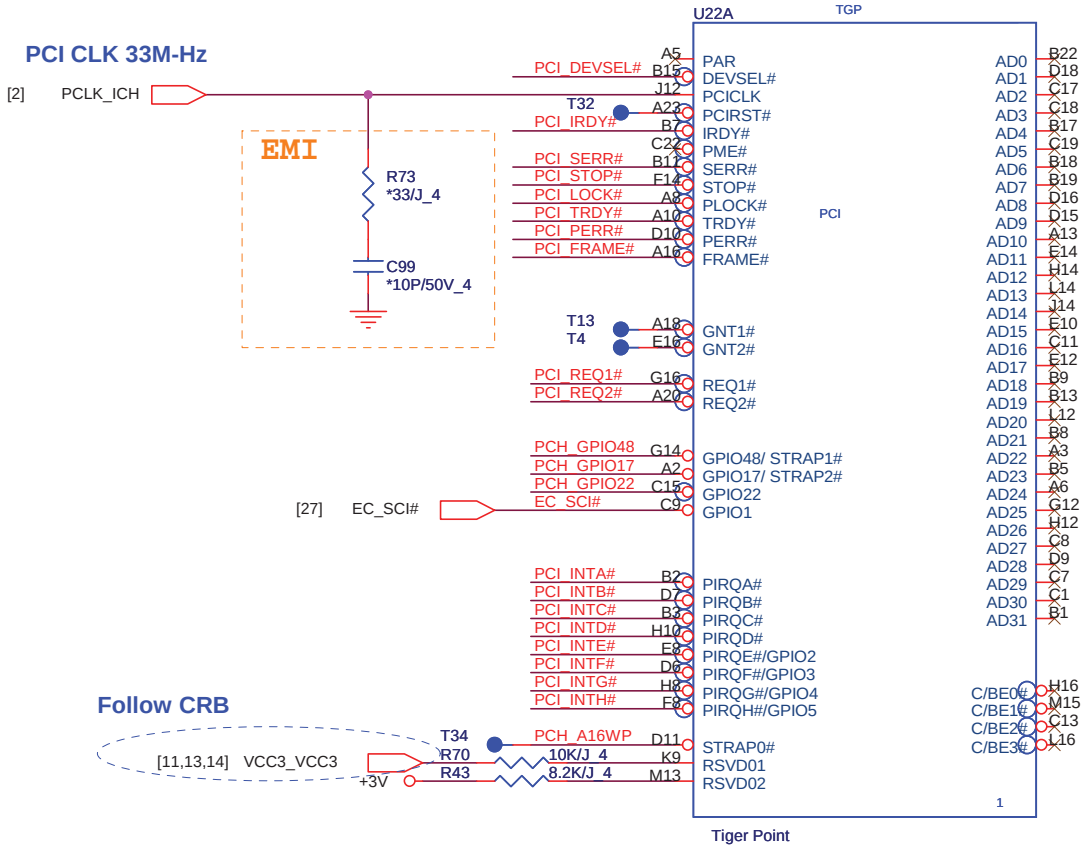
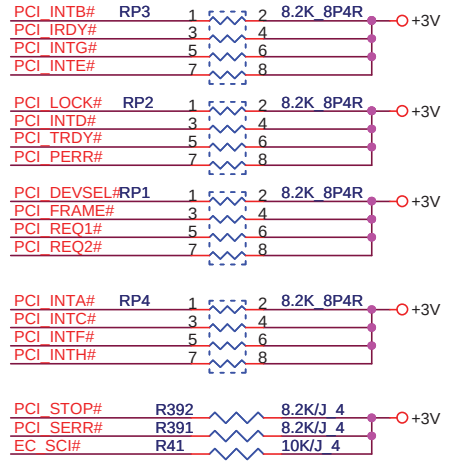
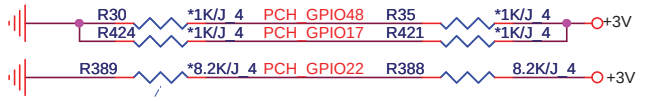
Tiger Point (CLG)







<20101104> Reserve R389(PCH_GPIO22 PD) for 27MHz or 96MHz choosing, need vBIOS support
Pull up --> for 27MHz
Pull down --> for 96MHz

<20090601(A1A)_Checklist Rev0.7>
Strap1#/strap2#: signals have weak internal pull-ups

ICH Boot BIOS select

PCH_GPIO17 (INT PU)	PCH_GPIO48 (INT PU)	Boot BIOS Location
0	1	SPI
1	0	PCI
1	***1***	***LPC (CURRENTLY USE)***

A16 SWAP Override strap

PCH_A16WP (INT PU)	Low = A16 swap override enabled High = Default

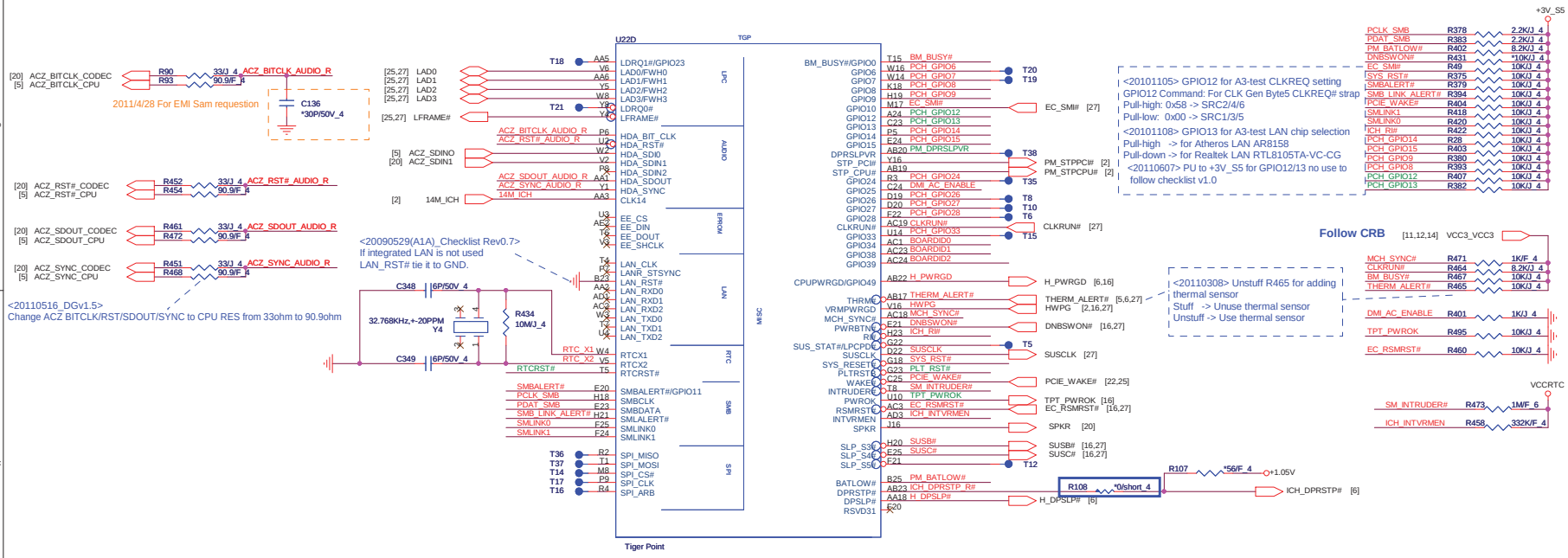
PCI_GNT#2	Internal PU Should not be PD

IRQ	Description
PIRQA	USB UHCI Controller #1, #4
PIRQB	AC'97 Codec; option for SMBUS
PIRQC	USB UH Controller #3; SATA/IDE Native Mode
PIRQD	USB UHCI Controller #2
PIRQE	Internal LAN; Option for SCI, TCO, HPET#0,1,2
PIRQF	Option for SCI, TCO, HPET#0,1,2
PIRQG	Option for SCI, TCO, HPET#0,1,2
PIRQH	USB EHCI Controller; Option for SCI, TCO, HPET#0,1,2

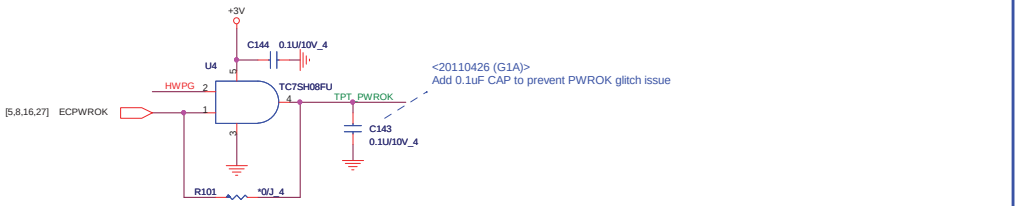
Quanta Computer Inc.
PROJECT : ZE7

Size	Document Number	Rev
	TigerPoint PCI	C3C
Date: Wednesday, August 31, 2011	Sheet 12 of 42	

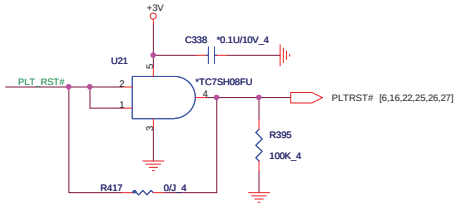
Tiger Point (CLG)



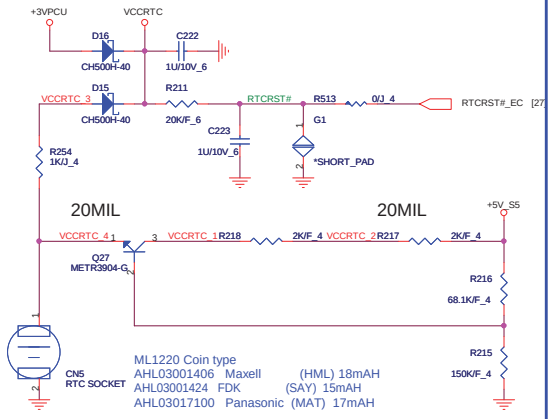
TPT Power OK (CLG)



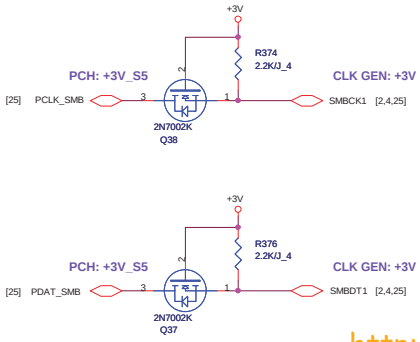
Platform Reset (CLG)



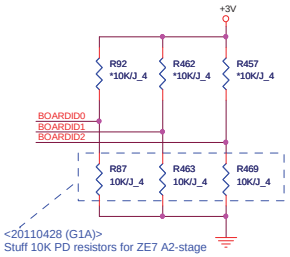
RTC (RTC)



Clock GEN I2C Level Shift



Mother Board ID (CLG)



ACZ_SDOUT (INT PD)	ACZ_SYNC (INT PD)	Description
0	**0**	*** 4 x 1s**
1	0	Reserved
0	1	Reserved
1	1	1 x 4s(1 port/4 lanes)

INTVRMEN	
1	Enable internal VccSus1_5 VRM (default)
0	Disable

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Size	Document Number	Rev
	TPT ACZ/GPIO/RTC	C3C

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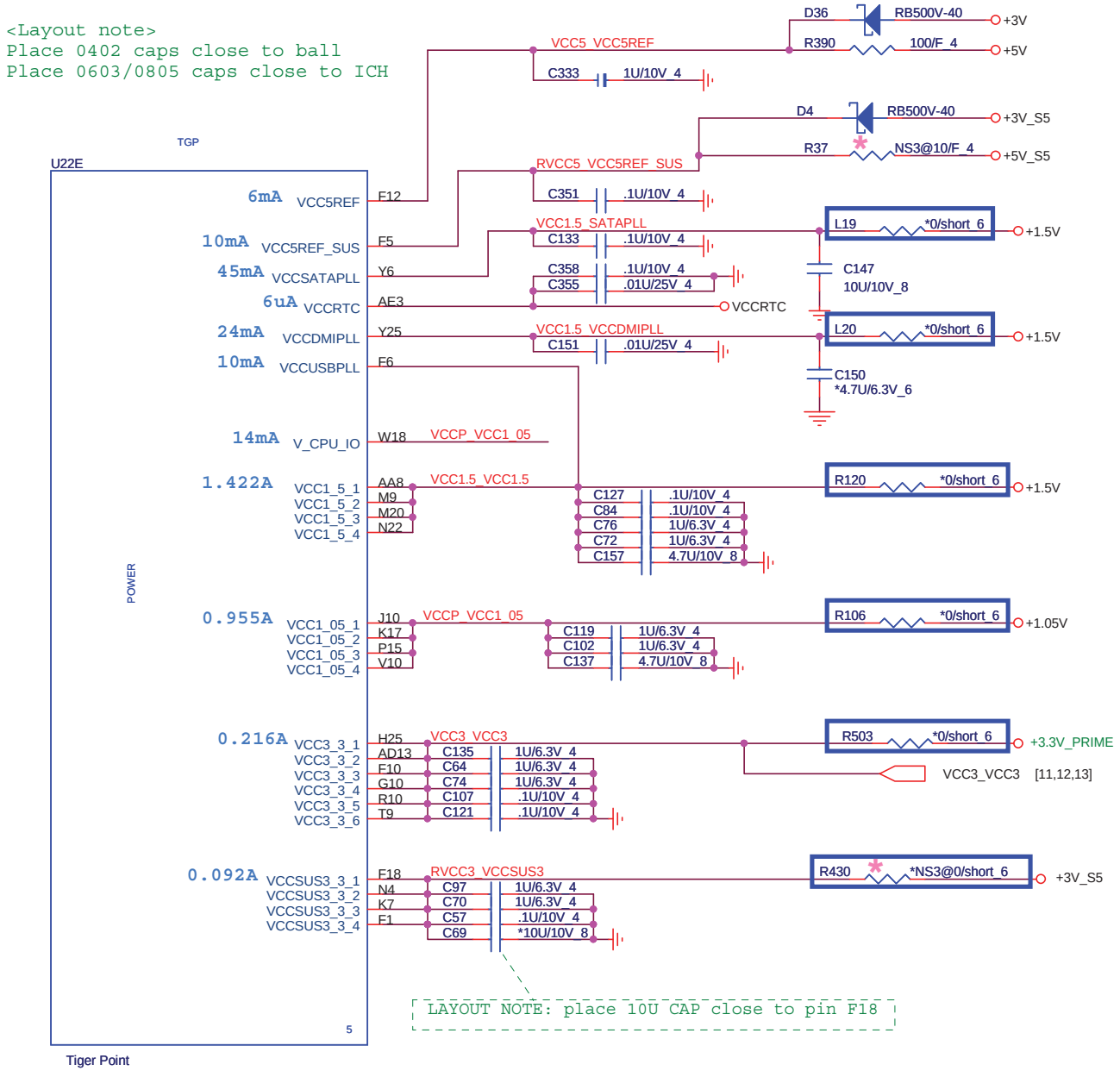
Tiger Point (CLG)

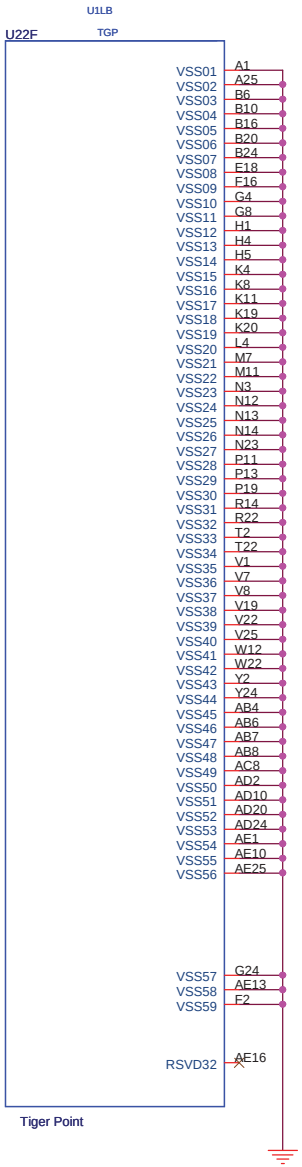


Quanta Computer Inc.

PROJECT : ZE7

Size	Document Number	Rev
	TigerPoint Power	C3C
Date: Wednesday, August 31, 2011	Sheet 14 of 42	

Tiger Point (CLG)



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PROJECT : ZE7		
Size	Document Number: TigerPoint GND	Rev: C3C
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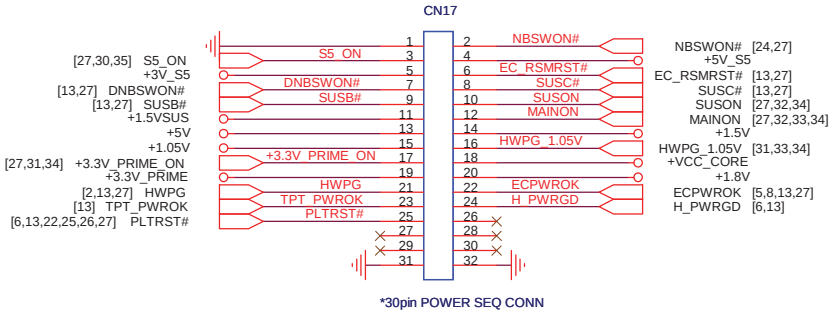
Power Sequence Connector 30pin (CPU)



*30pin POWER SEQ CONN

1	GND	11	+1.5VSUS	21	HWPG
2	NBSWON#	12	MAINON	22	ECPWROK
3	S5_ON	13	+5V	23	TPT_PWROK
4	+5V_S5	14	+1.5V	24	H_PWRGD
5	+3V_S5	15	+1.05V	25	PLTRST#
6	RSMRST#	16	HWPG_1.05V	26	RESERVE
7	DNBSWON#	17	VRON	27	RESERVE
8	SUSC#	18	+VCC_CORE	28	RESERVE
9	SUSB#	19	+3.3V_PRIME	29	RESERVE
10	SUSON	20	+1.8V	30	RESERVE

Quanta Computer Inc.

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Size	Document Number	Rev
	Cedarview XDP	C3C

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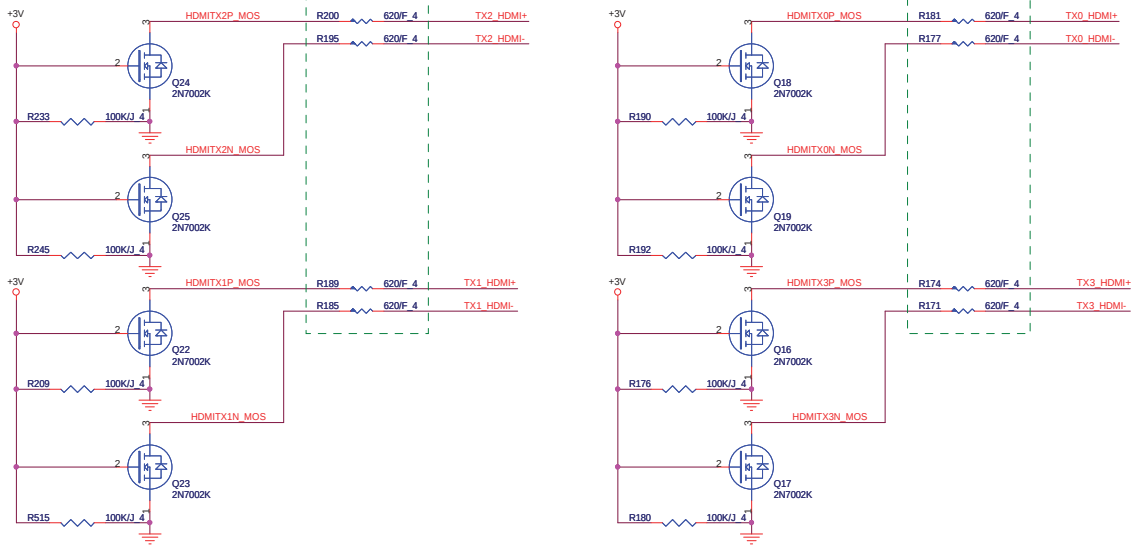
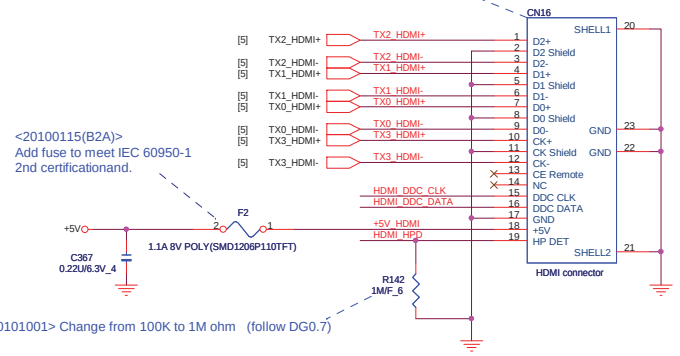
HDMI (HDM)

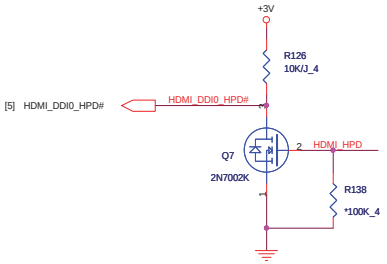
Level Shifter motherboard topology for max data rate of 1.65Gb/s

Close to HDMI connector



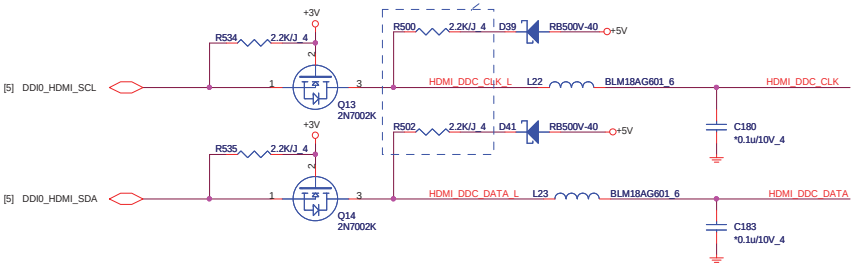
<20101209> Change to DFHS19FR015 by ME design change





SDVO I2C Control (HDM)

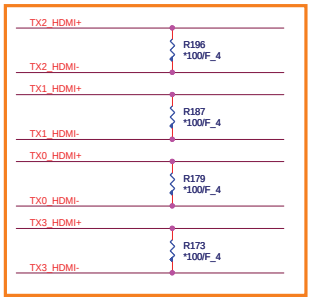
<20100909_Jennifer> Change R500/ R502 from 1.5k to 2.2k to follow CRB.



The DDC signals are rated at 5V at connector. The passgate can also be used to protect against back-power
when computer is OFF but the display is ON and still pulled up to 5 V.

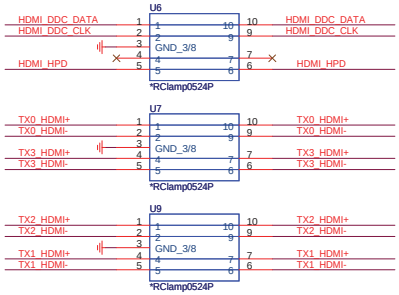
EMI reserve for HDMI (EMC)

Close to HDMI Connector



ESD Protect (HDM)

Close to HDMI Connector



Quanta Computer Inc.

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Size	Document Number	Rev
	HDMI	C3C

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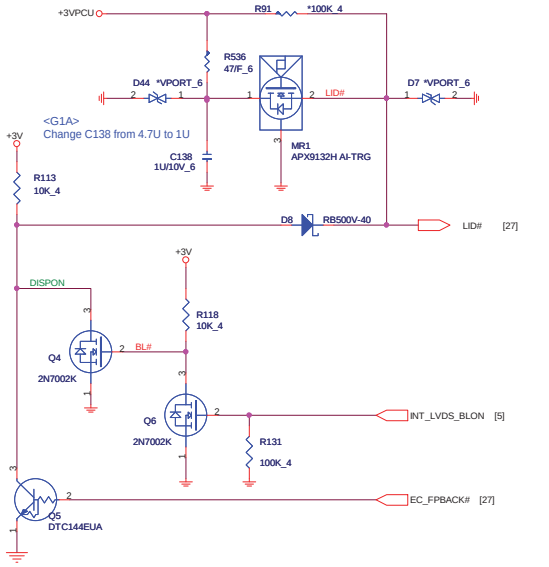
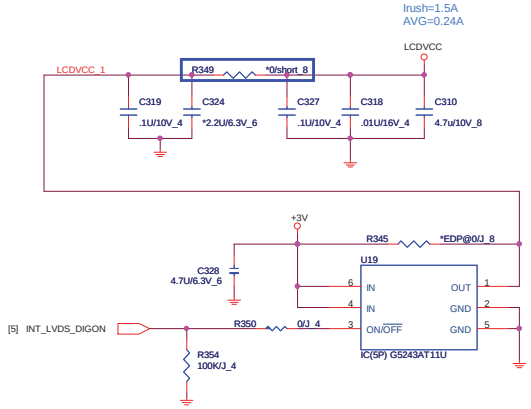
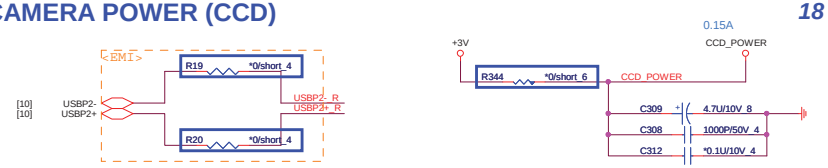
HALL IC (HSR)



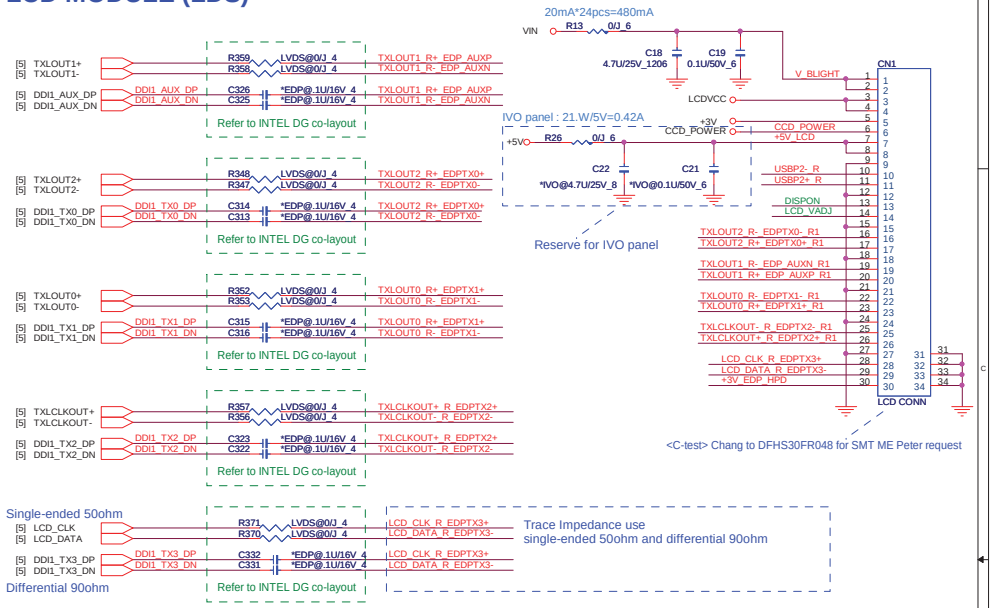
LCD POWER SWITCH (LDS)



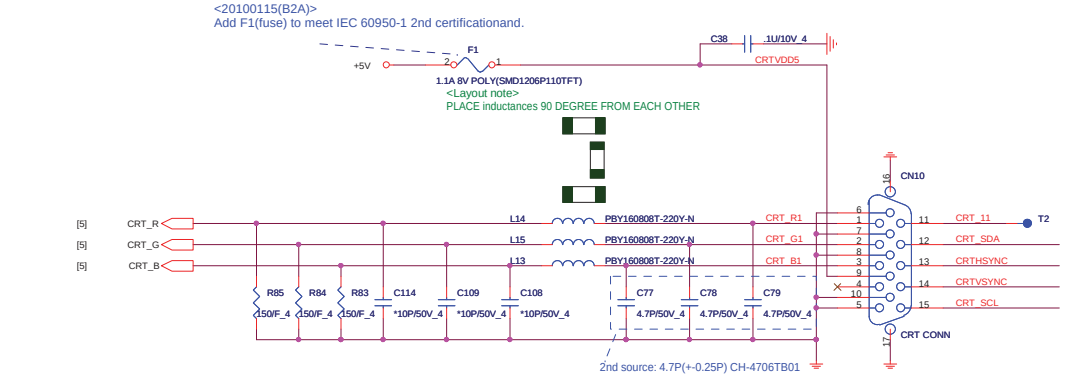
CAMERA POWER (CCD)

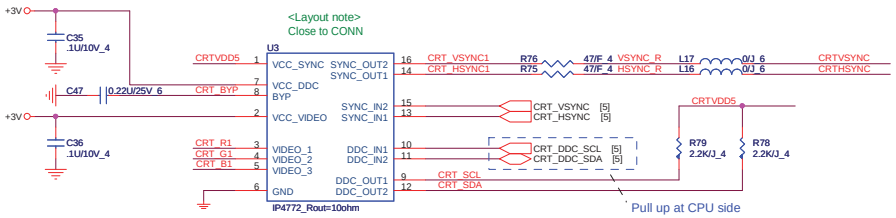


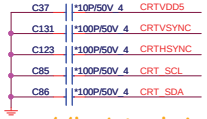
LCD MODULE (LDS)



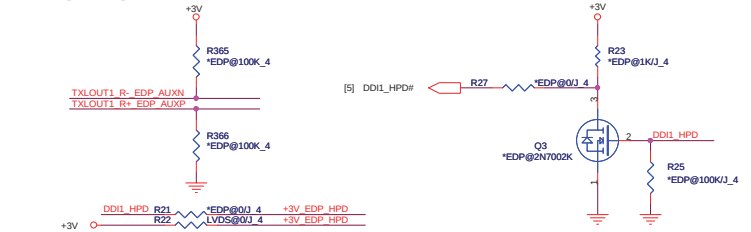
CRT(CRT)

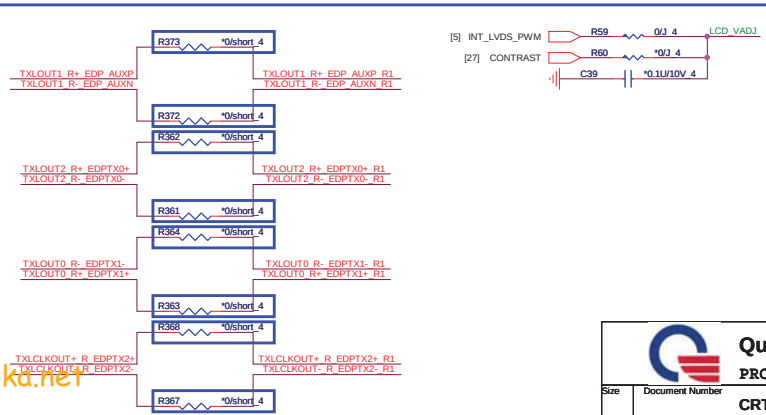






eDP (LDS)





Quanta Computer Inc.
PROJECT : ZE7

Size	Document Number	Rev
	CRT/LVDS/EDP	C3C

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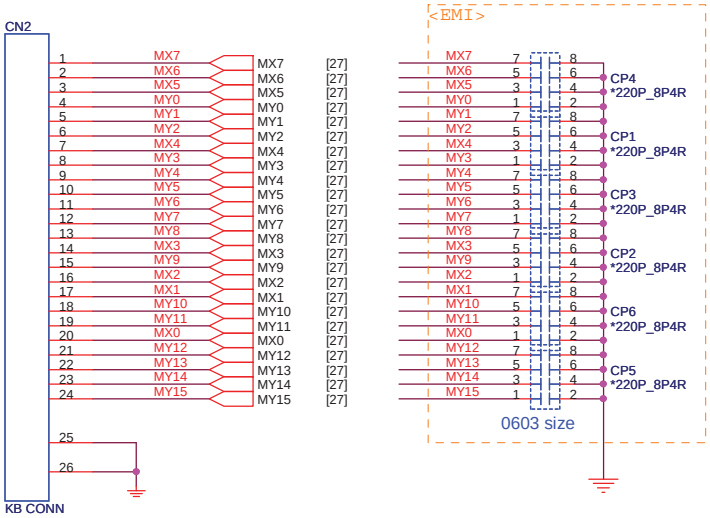
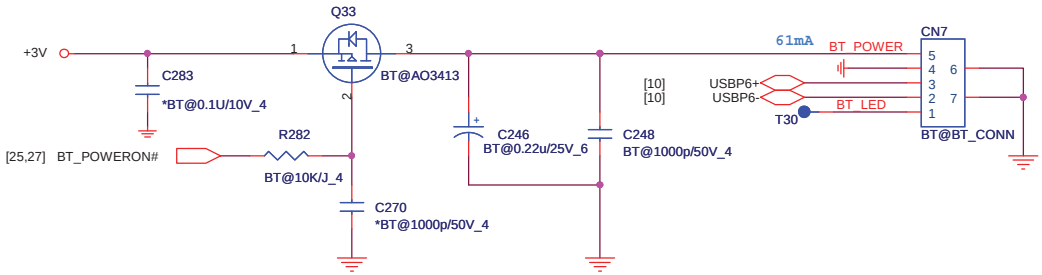
KEYBOARD (KBC)

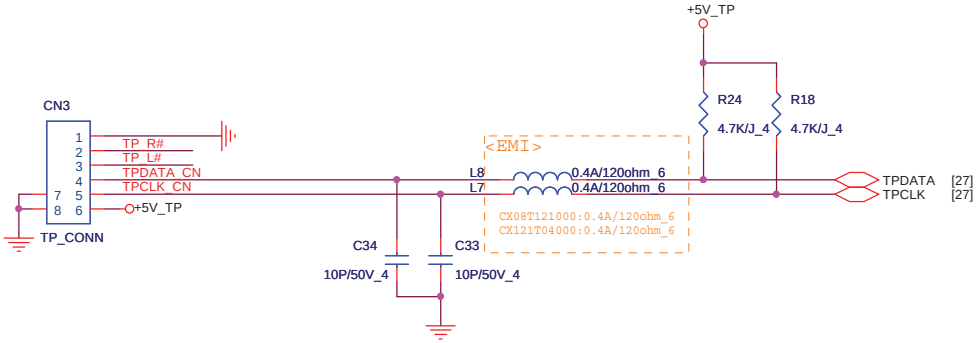
<20110214(E1A)>
Change CP1~CP6 footprint from
8p4r-0402-smt to 8P4R, for SMT open issue.



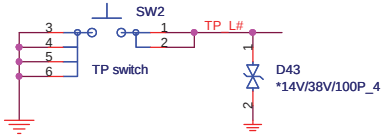
BLUETOOTH (BTM)



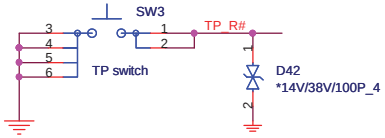
TOUCH PAD (TPD)

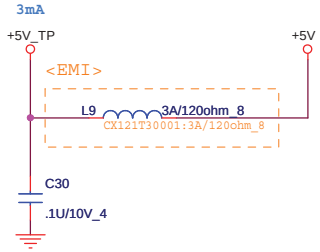


Left Button



Right Button





Quanta Computer Inc.
PROJECT : ZE7

Size	Document Number	Rev
	KB/BT/TP/LED/Power Connector	C3C
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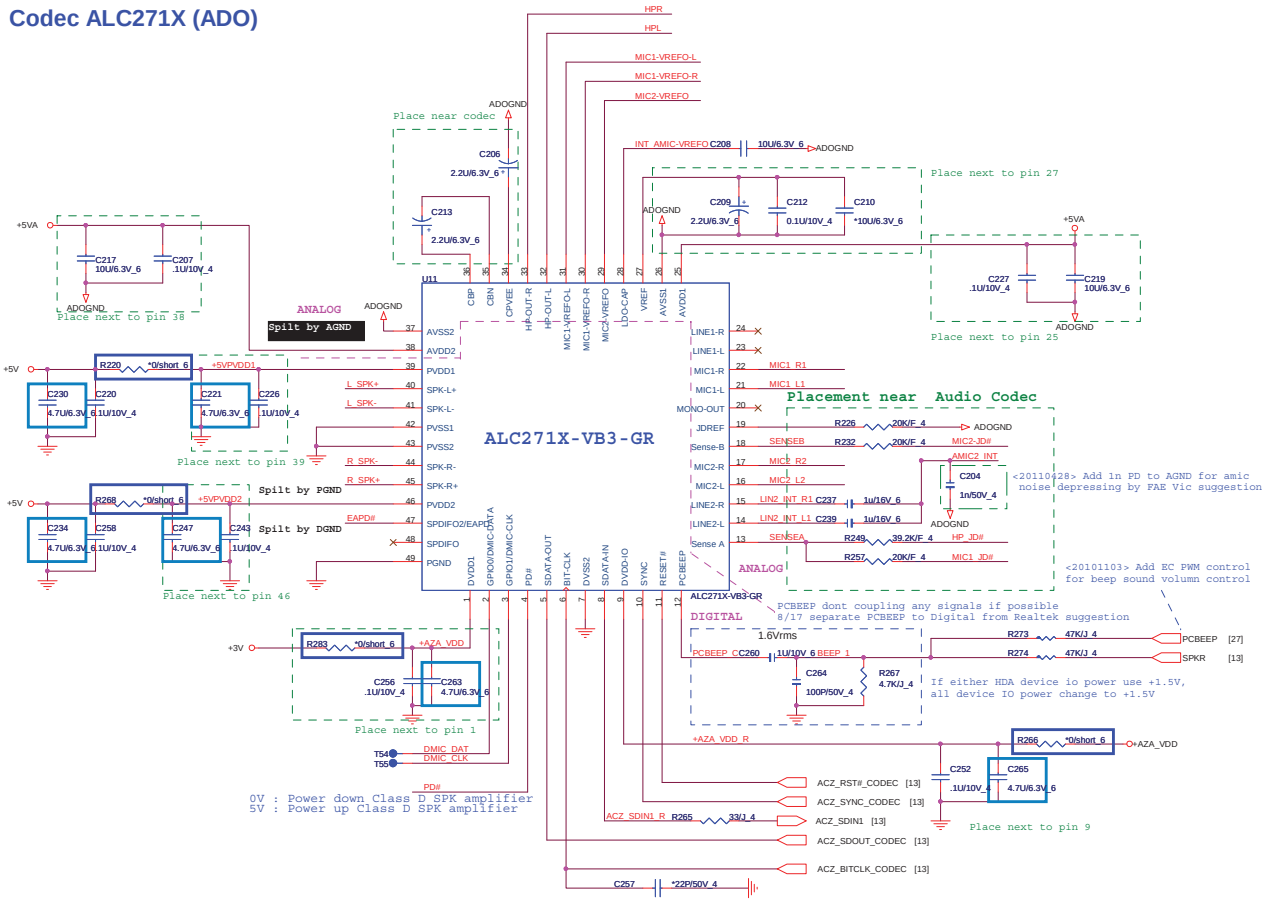
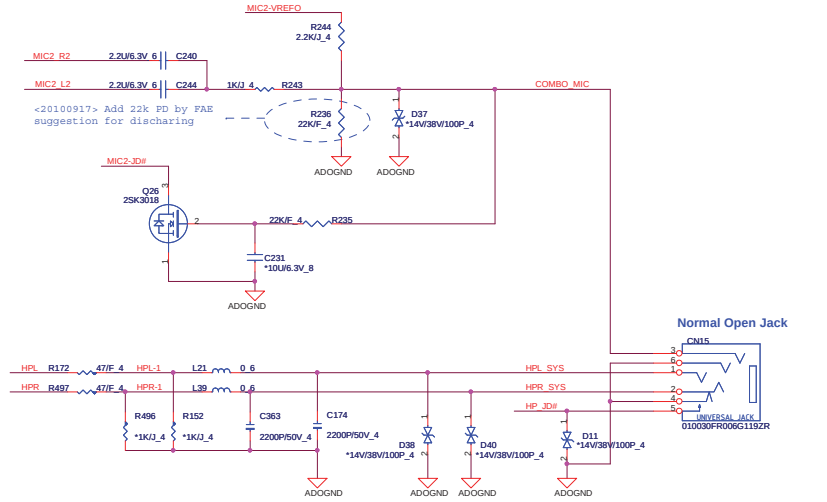
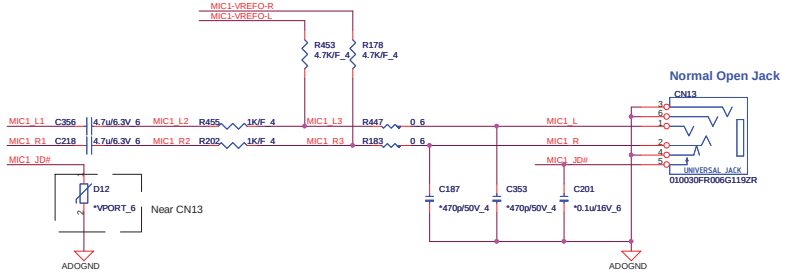
Codec ALC271X (ADO)



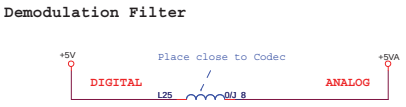
EARPHONE (AMP)



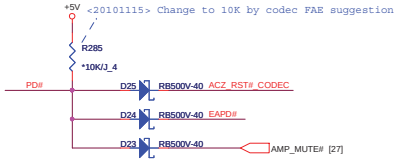
MIC (AMP)



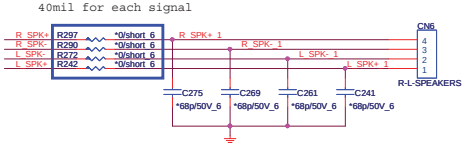
Power (ADO)



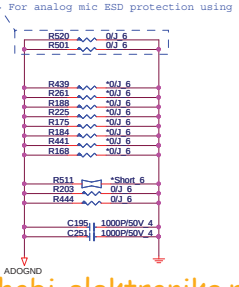
Mute (ADO)



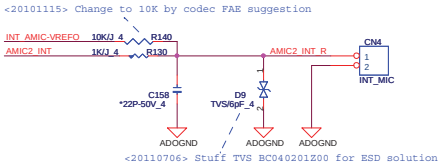
Internal Speaker (AMP)



GND



Internal Analog MIC (AMP)



Quanta Computer Inc.
PROJECT : ZE7

Size	Document Number	Rev
	ALC271X / AMP / SPK	C3C
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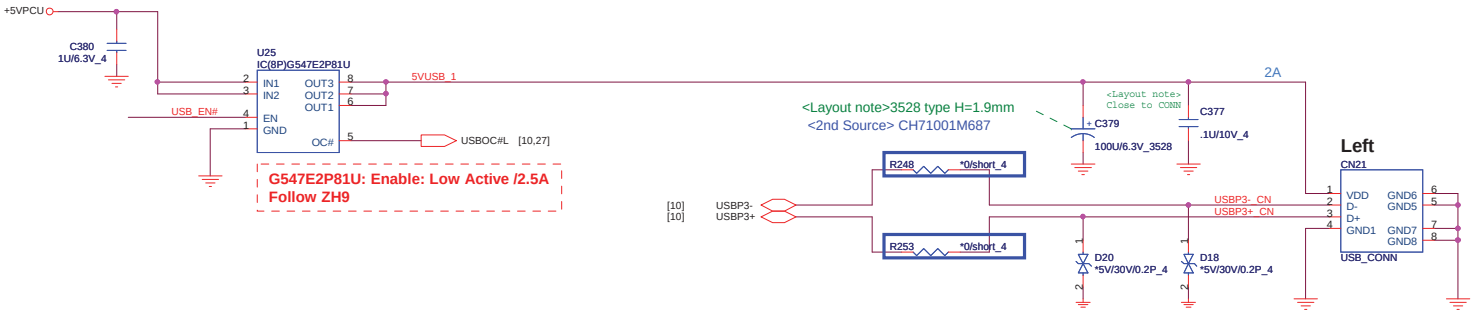
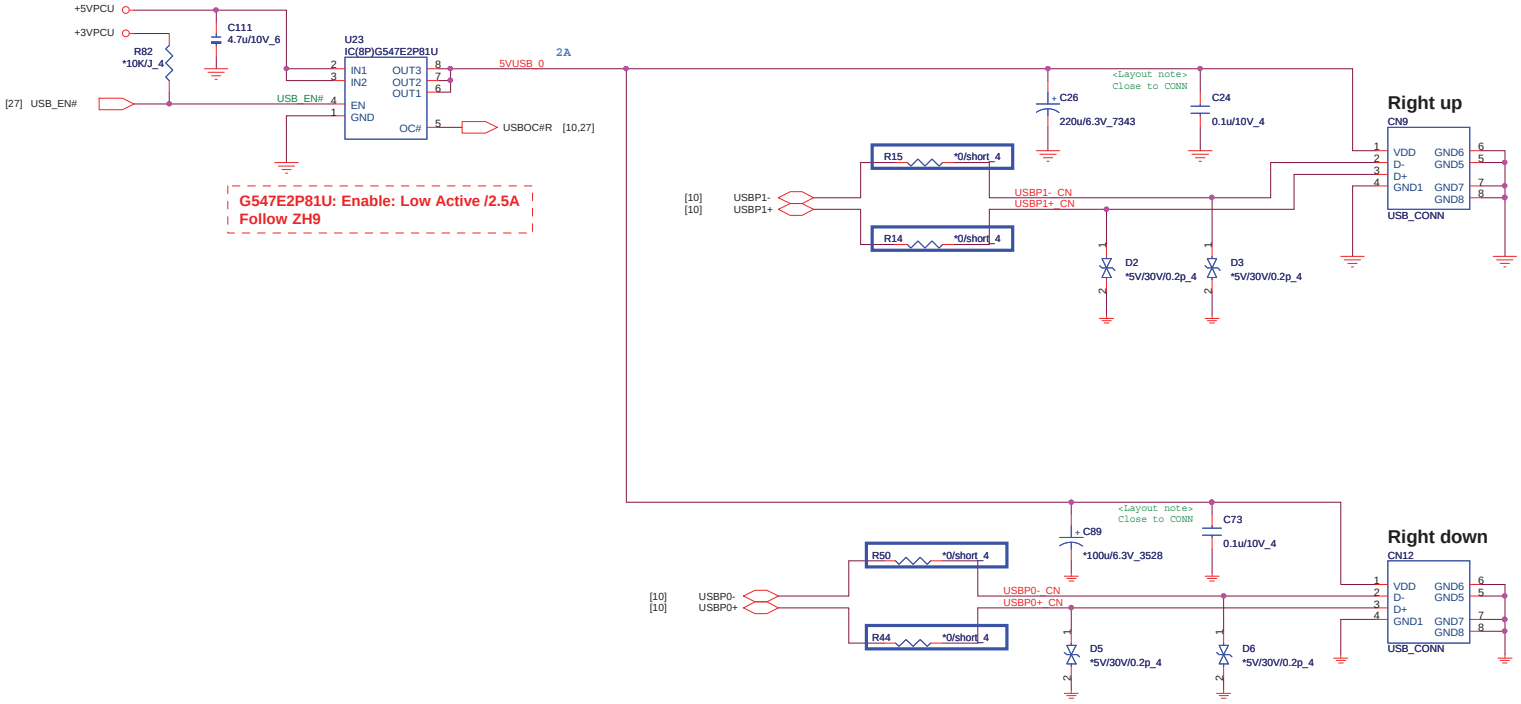
USB Left (USB)



USB Right (USB)



Quanta Computer Inc.

PROJECT : ZE7

Size	Document Number	Rev
	USB Port/ MAX14566EETA	C3C
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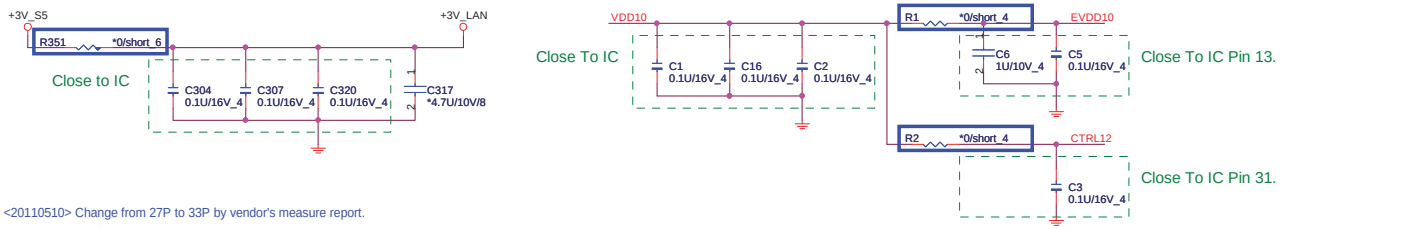
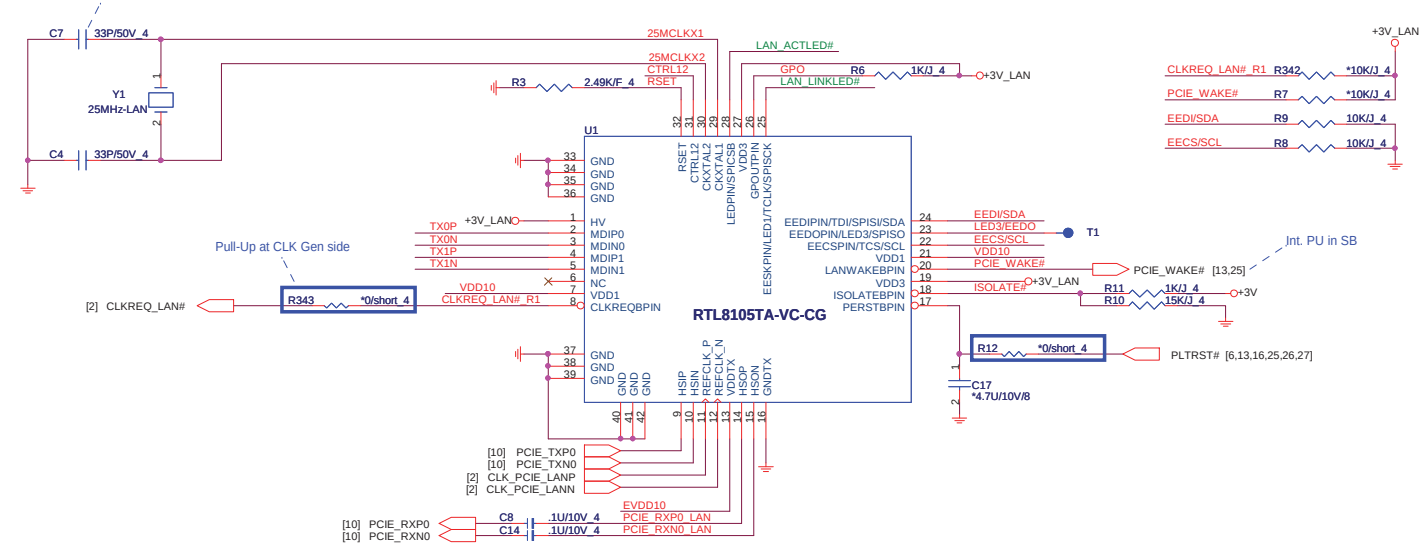
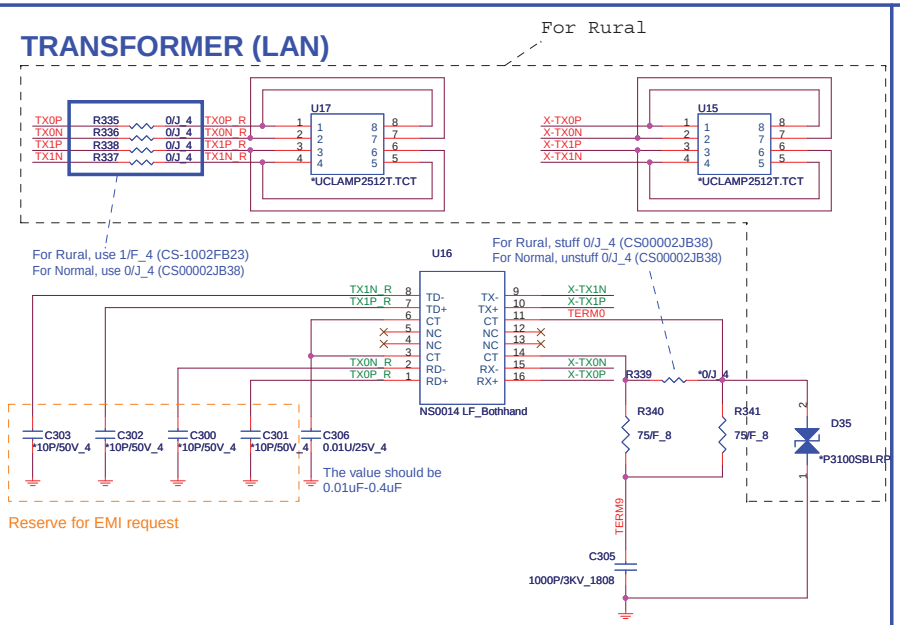
LAN (LAN)



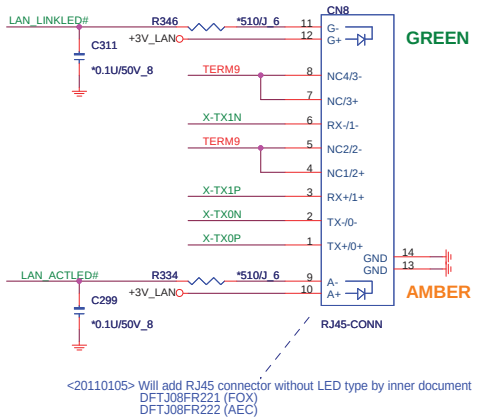
<20110510> Change from 27P to 33P by vendor's measure report.



TRANSFORMER (LAN)



RJ45 Connector (LAN)



<20110105> Will add RJ45 connector without LED type by inner document
DFTJ08FR221 (FOX)
DFTJ08FR222 (AEC)

Quanta Computer Inc.
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Size: Document Number: LAN RTL8105TA-VC-CG Rev: C3C
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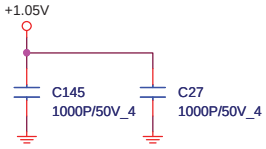
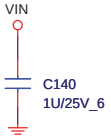
Stitching Capacitor (CLG)

For RF Request



For CRT R/G/B Signals



Quanta Computer Inc.		
PROJECT : ZE7		
Size	Document Number: Stitching Cap	Rev: C3C
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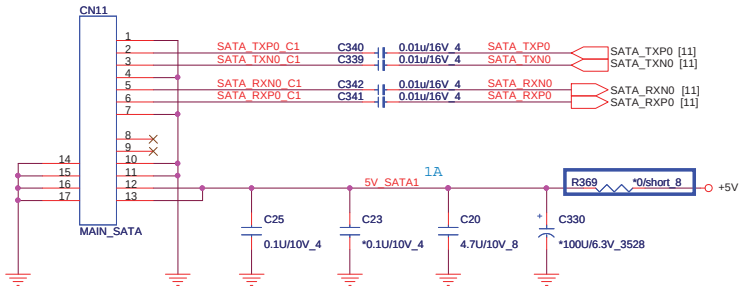
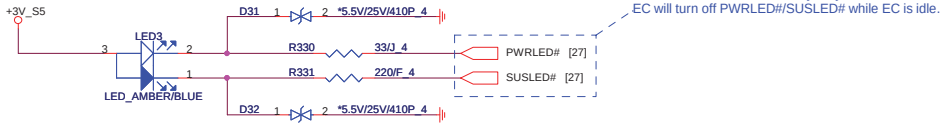
2.5" SATA HDD (HDD)



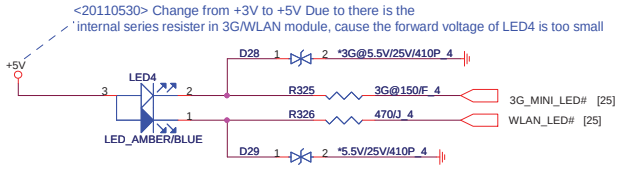
LED/SW (UIF)

PWR LED
SUS LED

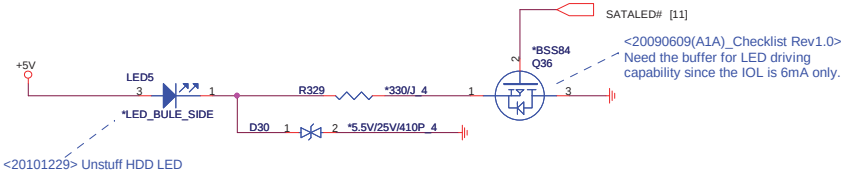


FULL LED
CHG LED

3G LED
WLAN LED

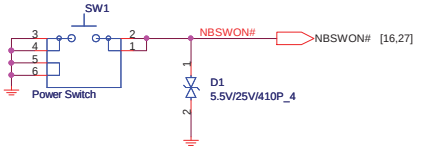


HDD LED



PWR indicator

PWR button



Quanta Computer Inc.		
PROJECT : ZE7		
Size	Document Number	Rev
	SATA HDD/LED/SW	C3C
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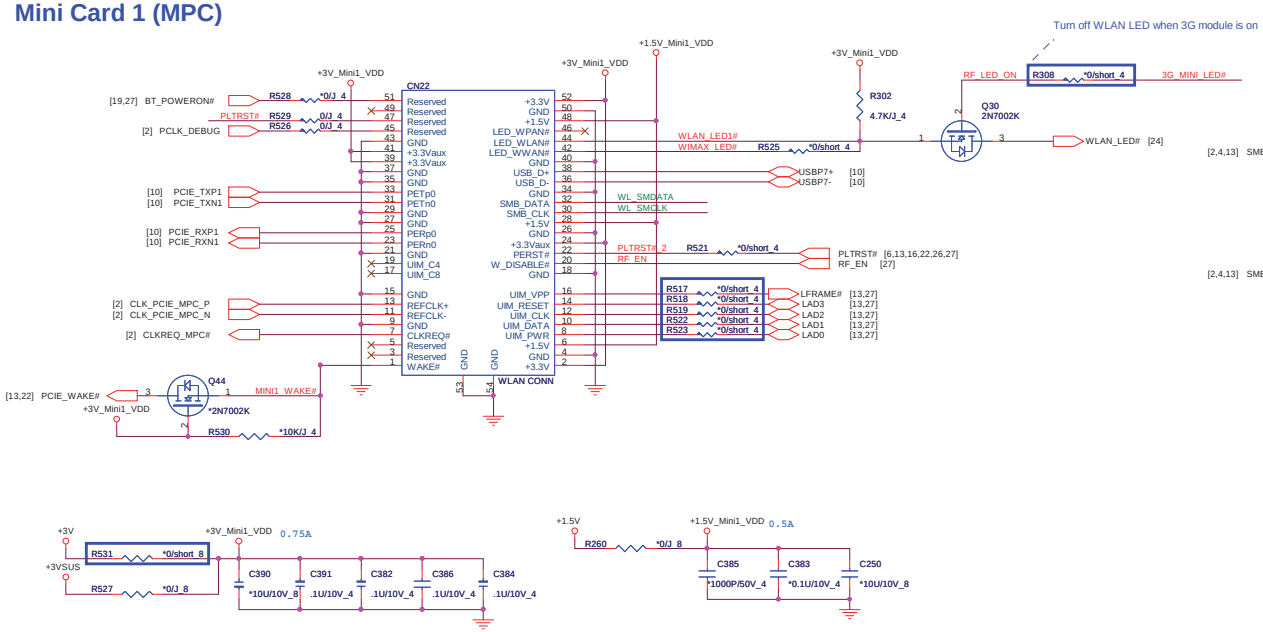
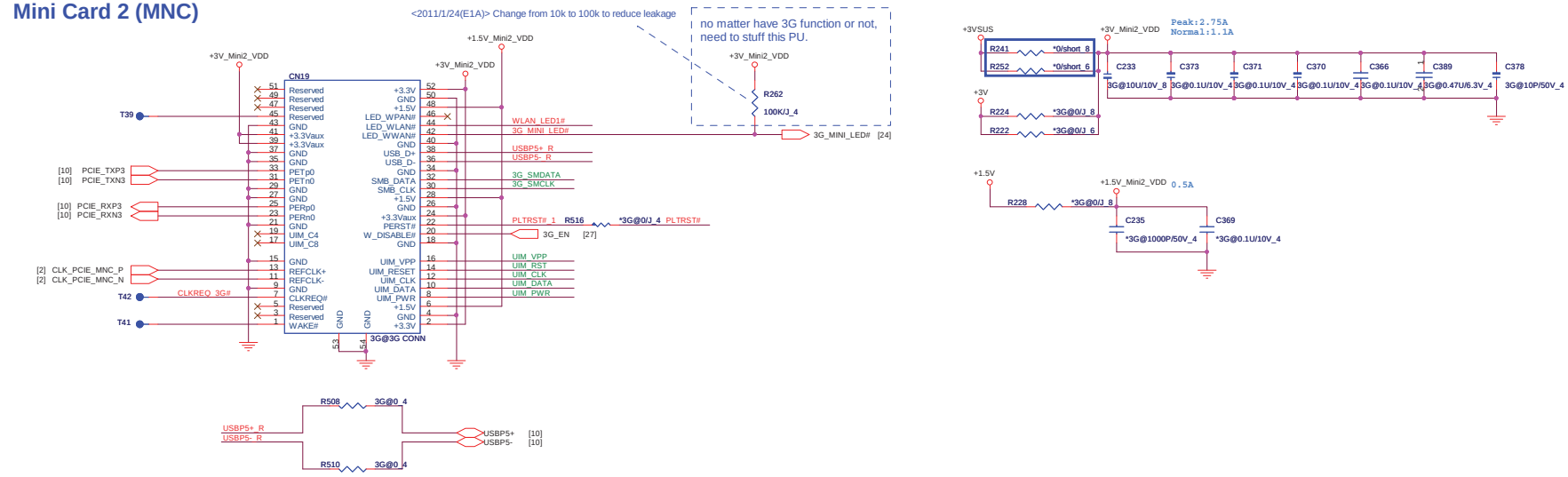
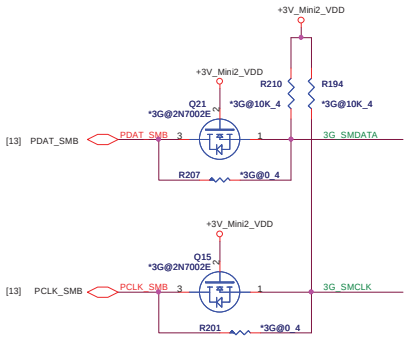
Mini Card 1 (MPC)

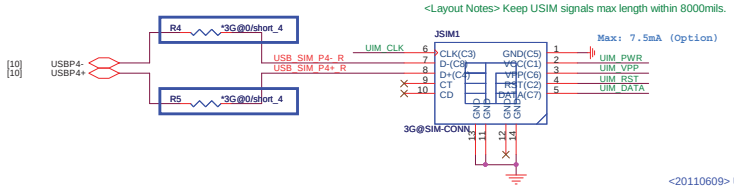


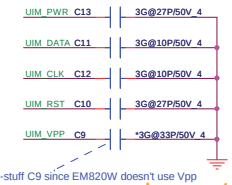
Mini Card 2 (MNC)



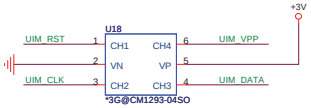


MultiMedia SIM (MNC)

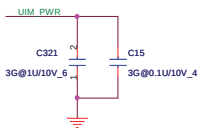




<20110609> Un-stuff C9 since EM820W doesn't use Vpp



<20090604(A1A)_Qualcomm design guide>
Place 0.1uF near connector's VCC pin



Quanta Computer Inc.
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Size	Document Number	Rev
	Mini-Card/WL/3G/SIM	C3C
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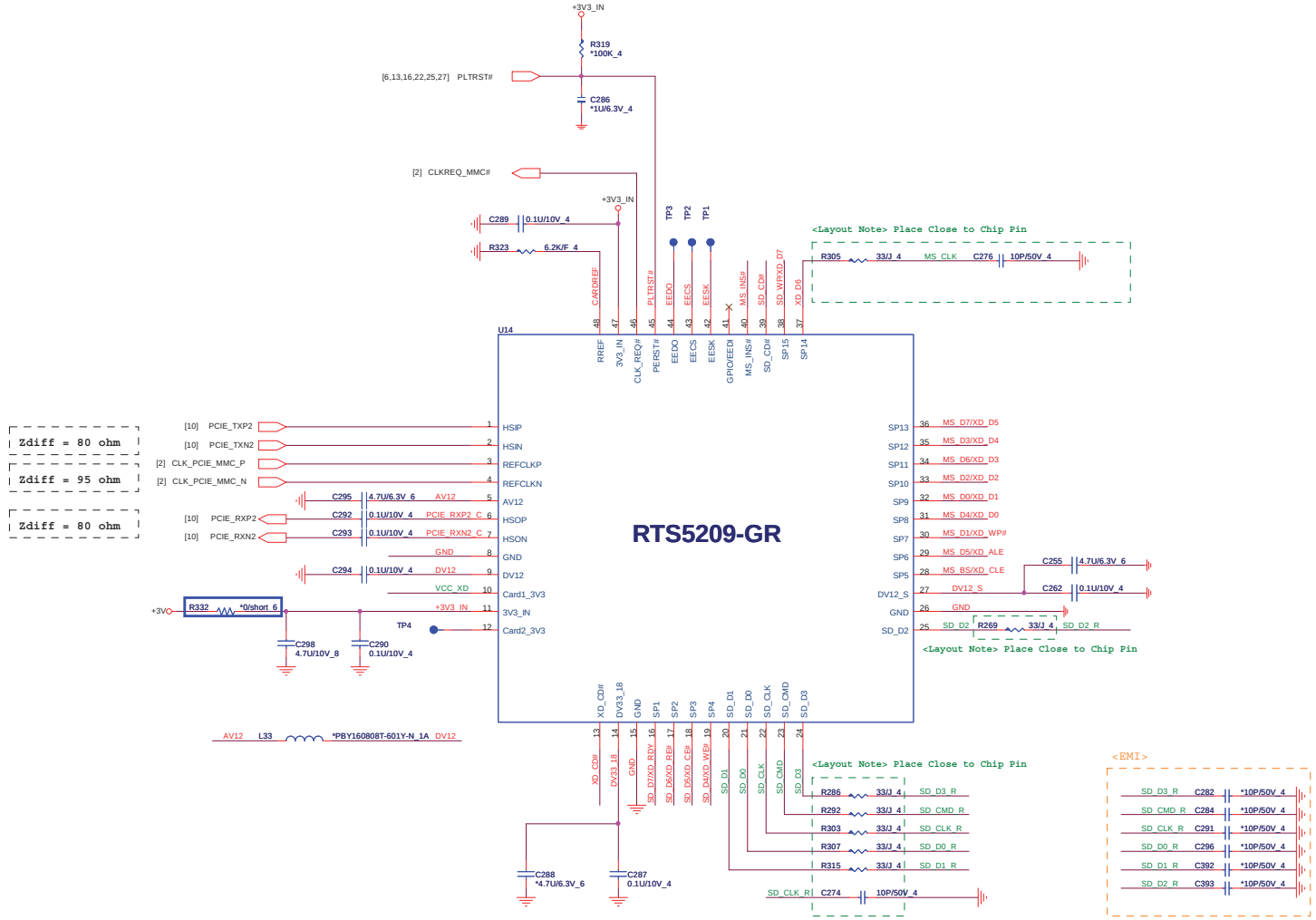
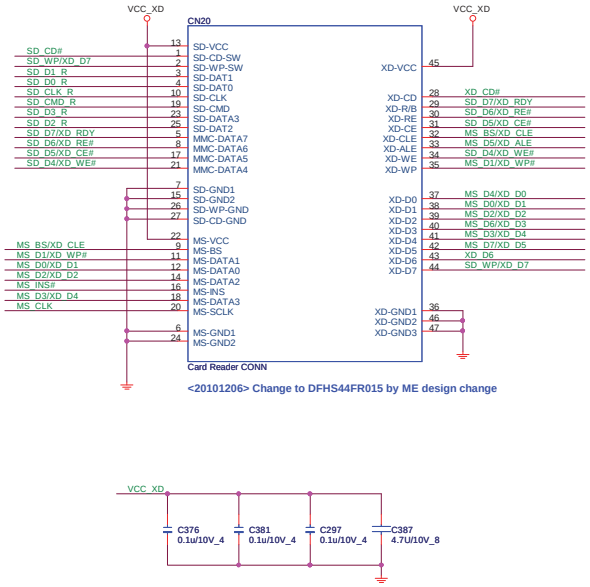
Card reader controller (MMC)



5 IN 1 Card Reader CONN (MMC)



Quanta Computer Inc.			
PROJECT : ZE7			
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	RTS5209-GR (Card Reader)		C3C
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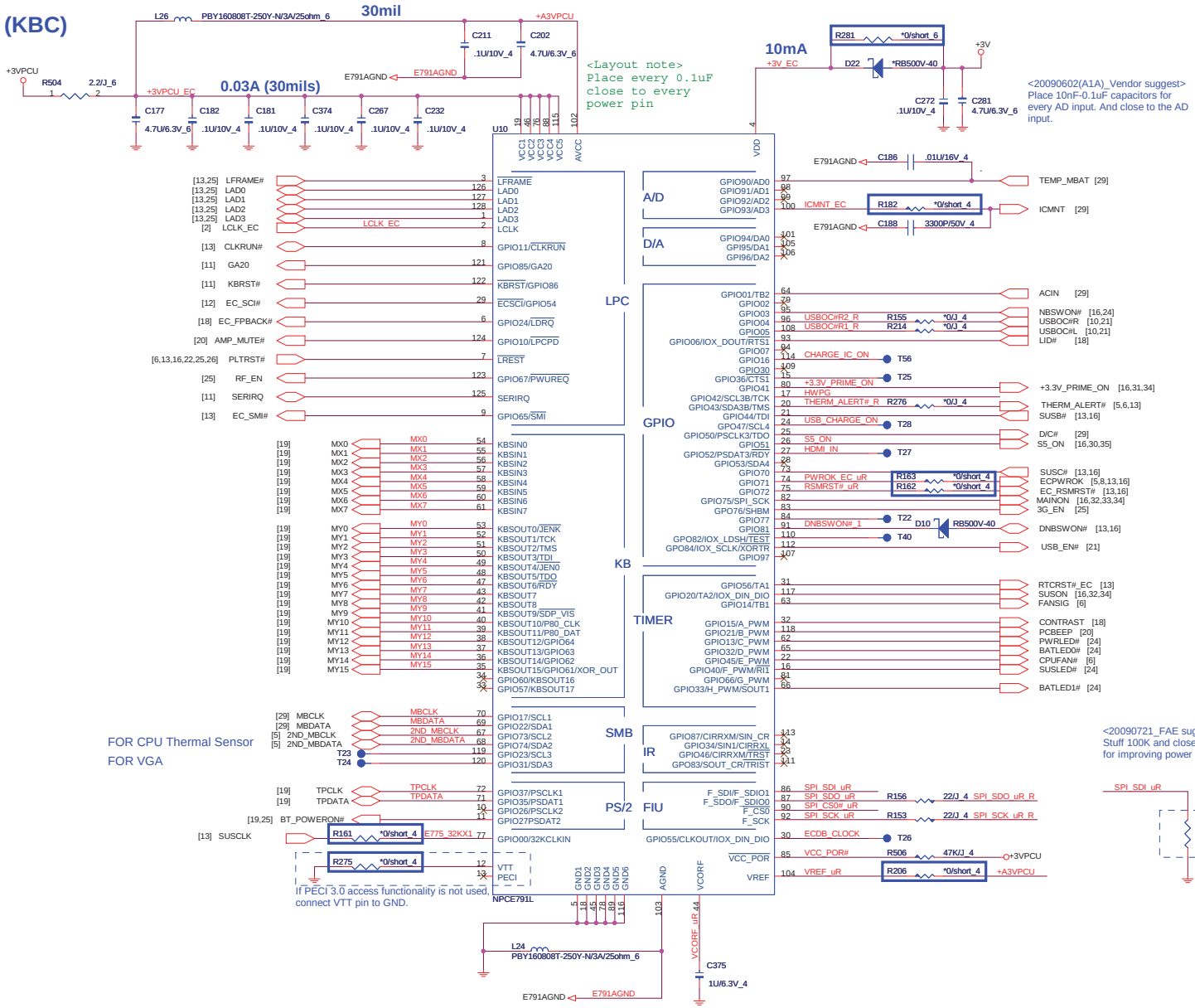
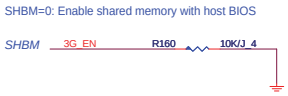
EC (KBC)



I/O ADDRESS SETTING(KBC)

SHBM=0: Enable shared memory with host BIOS



1/13 Comfirm by vendor mail :
Disabled ('1') if using FWH device on LPC.
Enabled ('0') if using SPI flash for both system BIOS and EC firmware

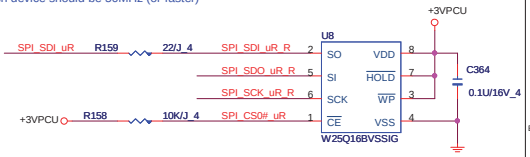
SM BUS PU(KBC)

1ST: Battery
2ND: CPU Thermal Sensor / DTS
3RD: VGA Thermal Sensor

<20090831(A1A)_EC team suggest>
1.change R166/R167 to 1M or 100K ohm
2.change PWR/SUS LED's power from +3VPCU to +3V_S5 or +3VSUS
can reduce pull-high resistor of SUSLED#/PWRLED#

SPI FLASH(KBC)

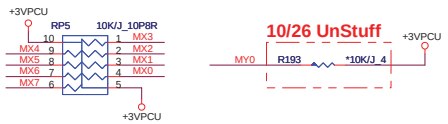
1/13 Comfirm by vendor mail :
If the Southbridge enables 'Long Wait Abort' by default, the
flash device should be 50MHz (or faster)



ZS9 A1~A3-test	W25Q16BVSSIG	AKE38FP0N01	16M bit
ZS9 A4-test	W25Q16CVSSIG	AKE38ZP0N02	16M bit
ZS9 A5-test	MX25L1606EM2I-12G	AKE38FP0Z01	16M bit
ZS9 A6-test	MX25L1606EM2I-12G	AKE38FP0Z01	16M bit
ZS9 A7-test	W25Q16BVSSIG	AKE38FP0N01	16M bit

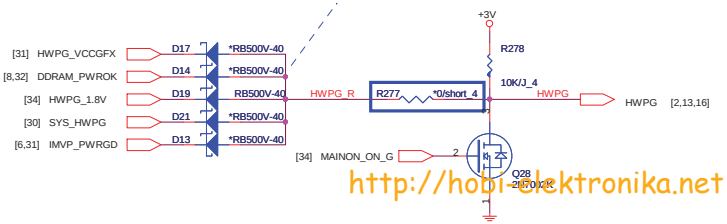
Winbond W25Q16BVSSIG AKE38FP0N01
EON EN25F16-75HCP AKE38ZA0Q00
MXIC MX25L1606EM2I-12G AKE38FP0Z01 (ZE6 MAC ID fail)

INTERNAL KEYBOARD STRIP SET (KBC)

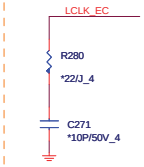


HWPG (KBC)

<20110829> DDRAM_PWROK no need connecting to EC side



<EMI>



Quanta Computer Inc.
PROJECT : ZE7

Size	Document Number	Rev
	NPCE791L & FLASH	C3C

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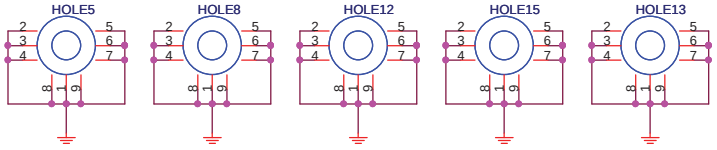
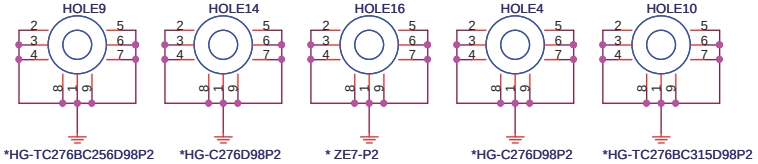
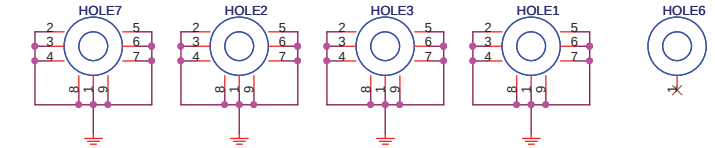
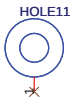
HOLE (OTH)

TOP(HDD Hole)

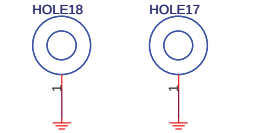




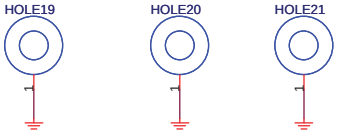




BOT(Thermal Hole)



BOT(Mini-PCIe Hole)



LED ESD PAD

TP ESD PAD

Quanta Computer Inc.

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Size	Document Number	Rev
	EMI/Hole	C3C
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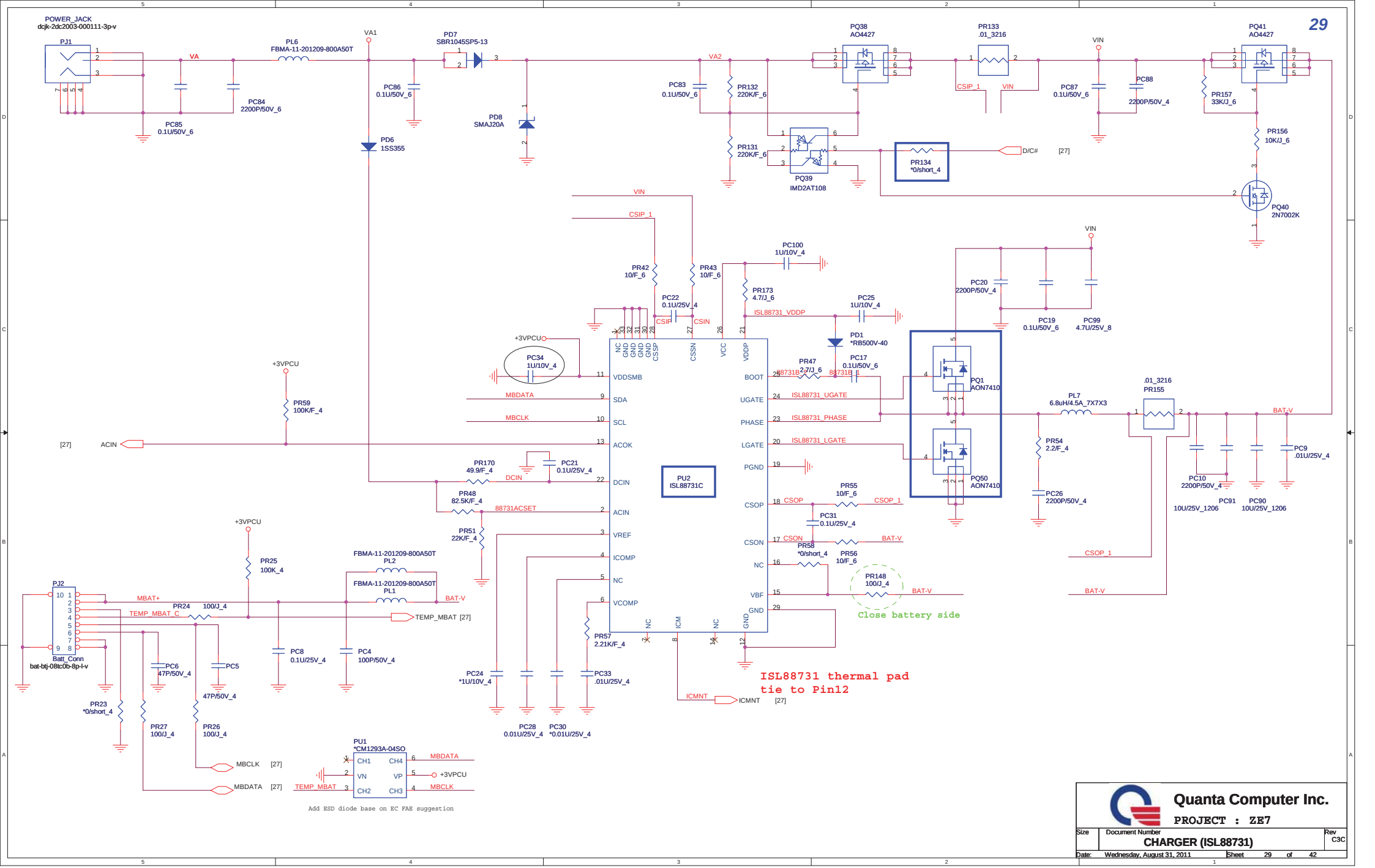

Quanta Computer Inc.		
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Size	Document Number: CHARGER (ISL88731)	Rev: C3C
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MAIND [32,34]
SUSD [34]
SYS_SHDN# [6,35]

[27] SYS_HWPG

+5VPCU
5 Volt +/- 5%
TDC : 4.858A
PEAK : 6.5A
OCP : 8A
Width : 200mil

+3VPCU
3 Volt +/- 5%
TDC : 2.368A
PEAK : 3.16A
OCP : 4A
Width : 100mil

PU3 RT8223M

OCP:8A
L(ripple current)
=(9-5)*5/(2.2u*0.4M*9)
=2.525A
Iocp=8-(2.525/2)=6.74A
Vth=6.74A*14mOhm=94.32mV
R(Ilim)=(94.32mV*10)/10uA
~94.32K

OCP:4A
L(ripple current)
=(9-3.3)*3.3/(2.2u*0.5M*9)
~1.9A
Iocp=4-(1.9/2)=3.05A
Vth=3.05A*14mOhm=42.7mV
R(Ilim)=(42.7mV*10)/10uA
=42.7K

PQ32 DTC144EU
PQ33 2N7002K
PQ16 2N7002K
PQ34 2N7002K
PQ35 AO3404
PQ12 AO3404
PQ22 AO3404
PQ15 AO3404
PQ24 AO3404

TDC : 0.008A
PEAK : 0.01A
Width : 10mil

TDC : 1.858A
PEAK : 2.477A
Width : 60mil

TDC : 1.03A
PEAK : 1.38A
Width : 50mil

TDC : 0.15A
PEAK : 0.2A
Width : 10mil

TDC : 0.94A
PEAK : 1.25A
Width : 40mil

Quanta Computer Inc.
PROJECT : ZE7
Size | Document Number: SYSTEM 5V/3V (RT8206) | Rev: C3C
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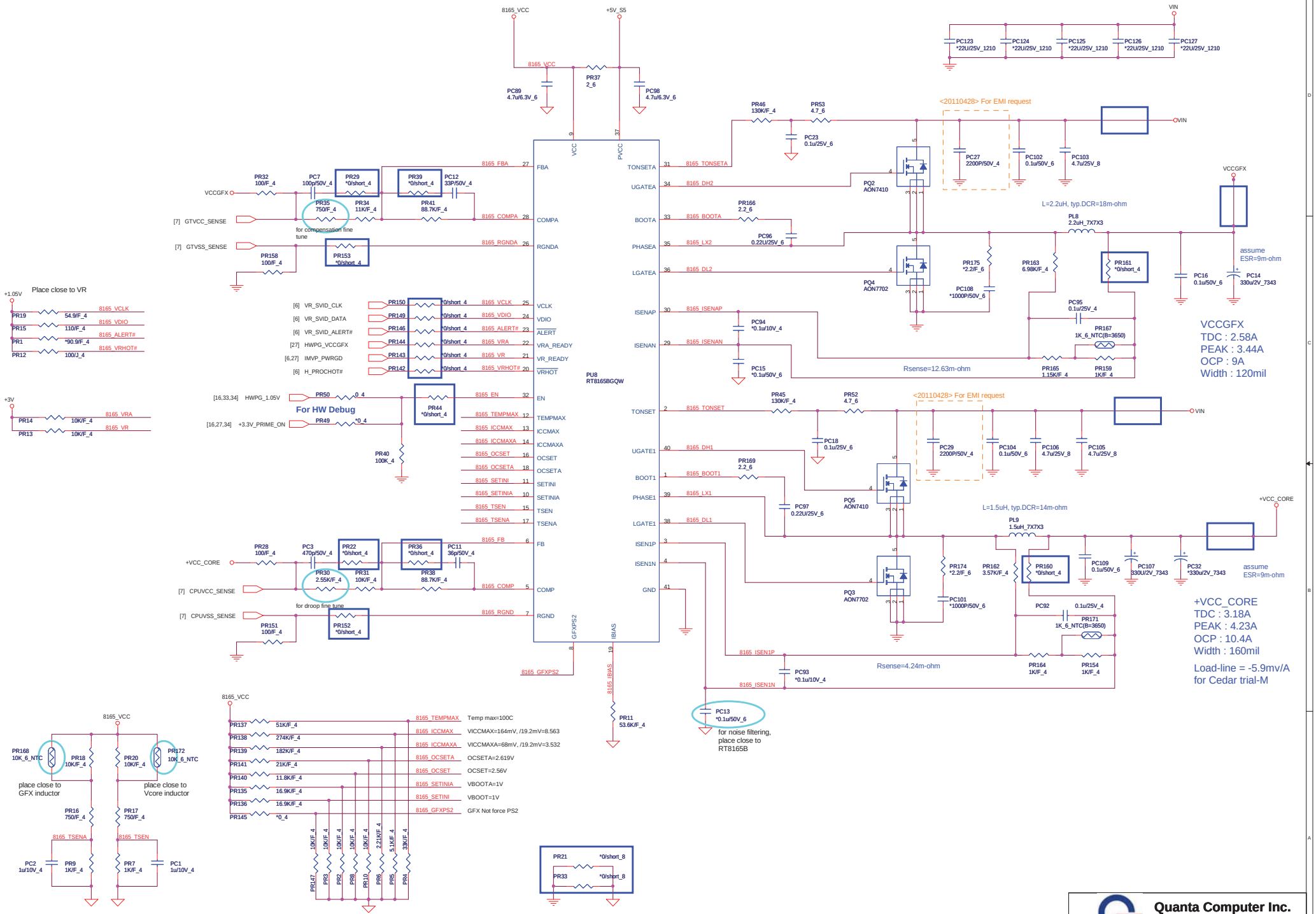

Quanta Computer Inc.
PROJECT : ZE7

Size	Document Number	Rev
	CPU CORE (RT8165B)	C3C
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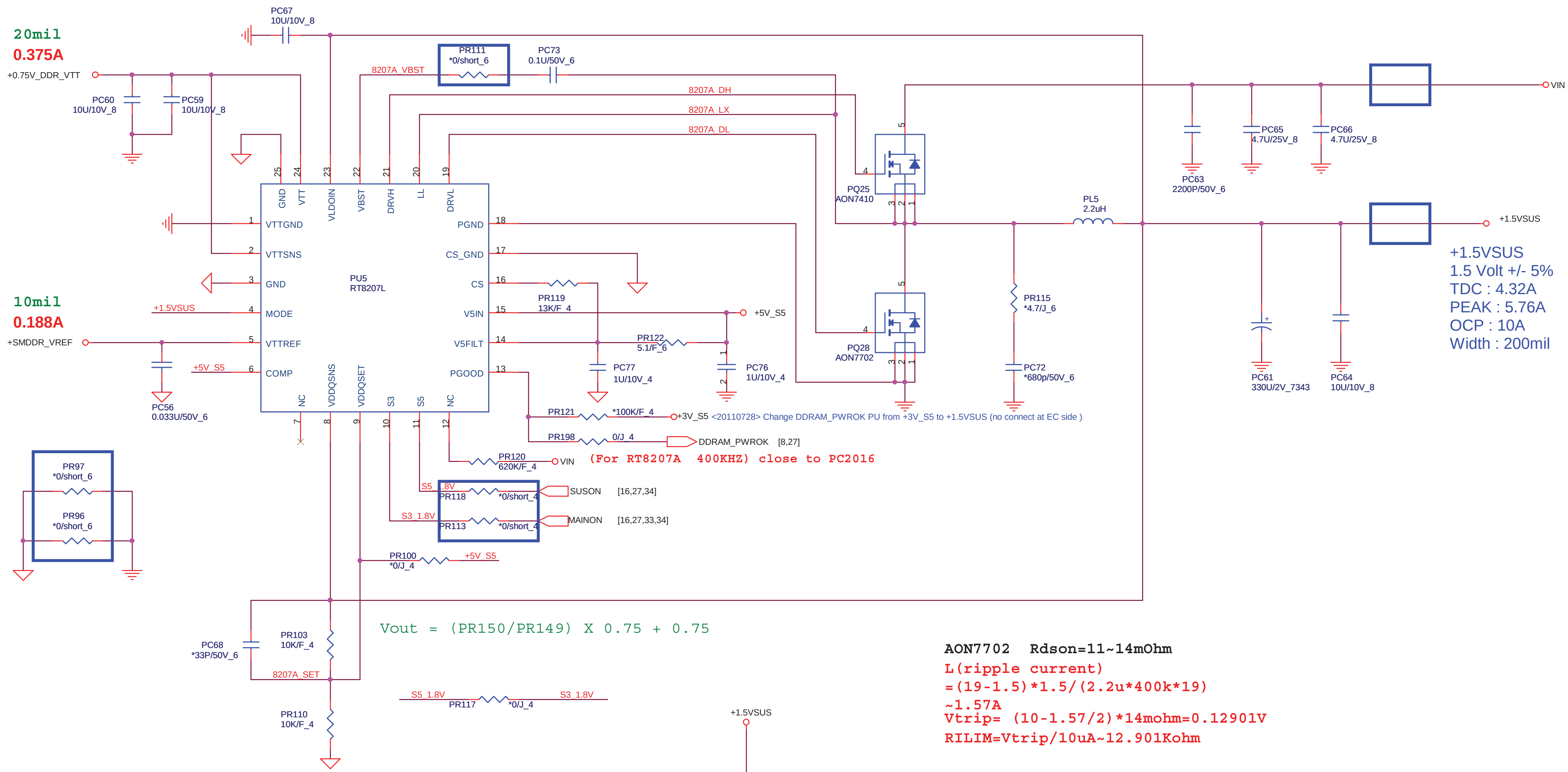
[PWM]



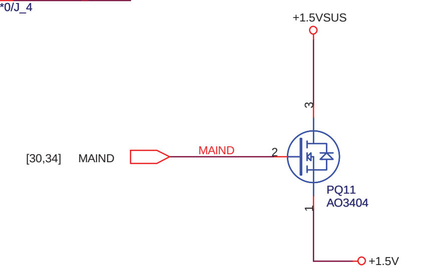
20mil
0.375A
+0.75V_DDR_VTT
PC60 10U/10V_8
PC59 10U/10V_8
PC67 10U/10V_8
PR111 *0/short_6
8207A_VBST
PC73 0.1U/50V_6
8207A_DH
8207A_LX
8207A_DL
PU5 RT8207L
VTTGND
VTTSNS
GND
MODE
VTTREF
COMP
VLDOIN
VBST
DRVH
LL
DRVL
VTT
PGND
CS_GND
CS
V5IN
V5FILT
PGOOD
NC
VDDQSNS
VDDQSET
S3
S5
10mil
0.188A
+1.5VSUS
+SMDDR_VREF
+5V_S5
PC56 0.033U/50V_6
PR119 13K/F_4
PR122 5.1/F_6
PC77 1U/10V_4
PC76 1U/10V_4
PQ25 AON7410
PQ28 AON7702
PR115 *4.7/J_6
PC72 *680p/50V_6
PL5 2.2uH
PC63 2200P/50V_6
PC65 4.7U/25V_8
PC66 4.7U/25V_8
VIN
+1.5VSUS
PC61 330U/2V_7343
PC64 10U/10V_8
+1.5VSUS
1.5 Volt +/- 5%
TDC : 4.32A
PEAK : 5.76A
OCP : 10A
Width : 200mil
PR121 *100K/F_4
+3V_S5 <20110728> Change DDRAM_PWROK PU from +3V_S5 to +1.5VSUS (no connect at EC side)
PR198 0/J_4
DDRAM_PWROK [8,27]
PR120 620K/F_4
VIN
(For RT8207A 400KHZ) close to PC2016
PR97 *0/short_6
PR96 *0/short_6
S5_1.8V
PR118 *0/short_4
SUSON [16,27,34]
S3_1.8V
PR113 *0/short_4
MAINON [16,27,33,34]
PR100 *0/J_4
+5V_S5
PC68 *33P/50V_6
PR103 10K/F_4
8207A_SET
PR110 10K/F_4
Vout = (PR150/PR149) X 0.75 + 0.75
S5_1.8V
PR117 *0/J_4
S3_1.8V

AON7702 Rdson=11~14mOhm

L(ripple current)
=(19-1.5)*1.5/(2.2u*400k*19)
~1.57A

Vtrip= (10-1.57/2)*14mohm=0.12901V

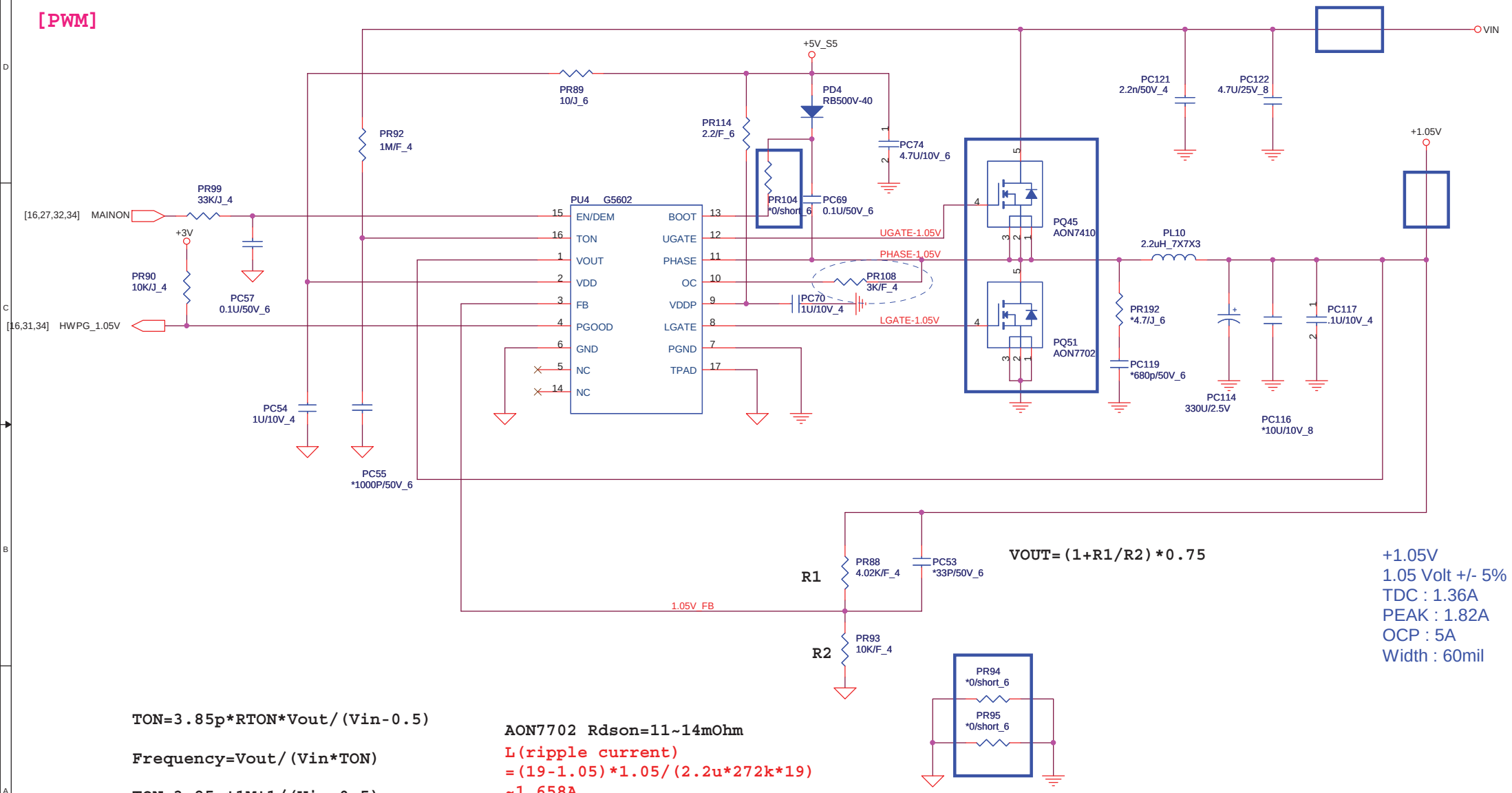
RILIM=Vtrip/10uA~12.901Kohm



TDC : 1.24A
PEAK : 1.65A
Width : 60mil

	S3	S5	+1.5VSUS	REF	VTT
S0	1	1	ON	ON	ON
S3	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF

[PWM]



VOUT=(1+R1/R2)*0.75

+1.05V
1.05 Volt +/- 5%
TDC : 1.36A
PEAK : 1.82A
OCP : 5A
Width : 60mil

TON=3.85p*RTON*Vout/(Vin-0.5)

Frequency=Vout/(Vin*TON)

TON=3.85p*1M*1/(Vin-0.5)

Frequency=1/(0.0036767)=272K

AON7702 Rdson=11~14mOhm

L(ripple current)
=(19-1.05)*1.05/(2.2u*272k*19)
~1.658A

Rth=14m*(5-0.829)/20uA

RILIM=2.92Kohm

Quanta Computer Inc.		
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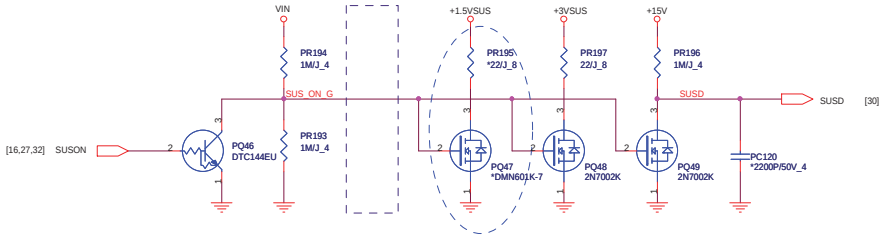
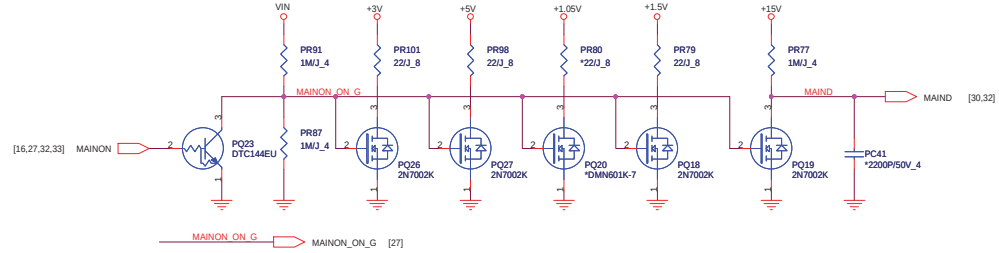
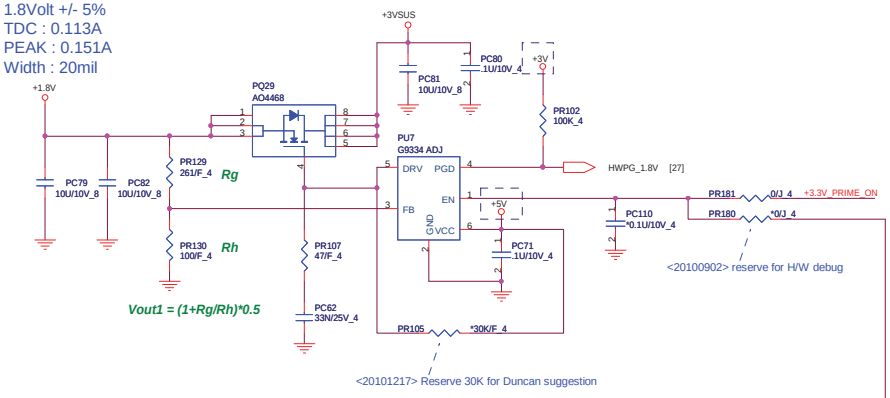


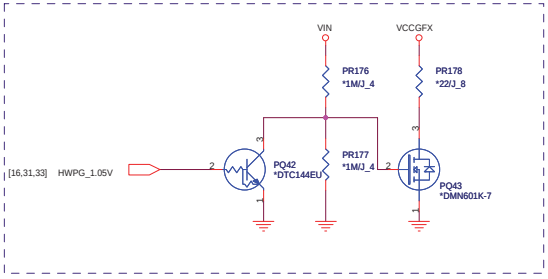


Reserve For VCCGFX

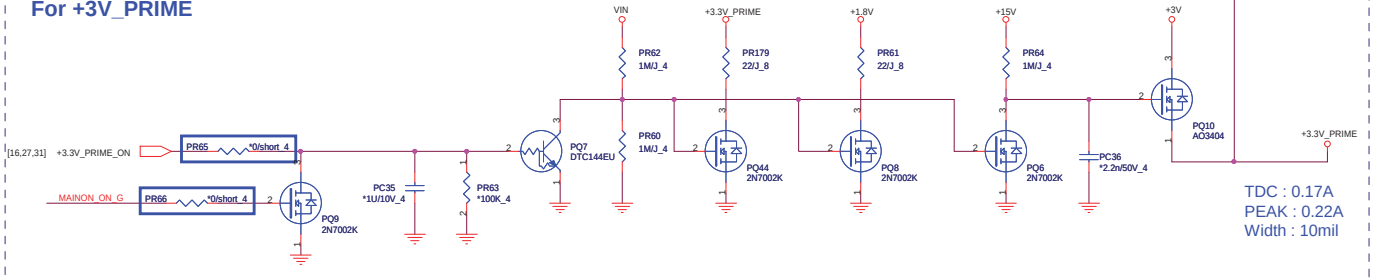
+1.8V
1.8Volt +/- 5%
TDC : 0.113A
PEAK : 0.151A
Width : 20mil



*Vout1 = (1+Rg/Rh)*0.5*



For +3V_PRIME



TDC : 0.17A
PEAK : 0.22A
Width : 10mil

Quanta Computer Inc.
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	Discharge/1.8V	C3C
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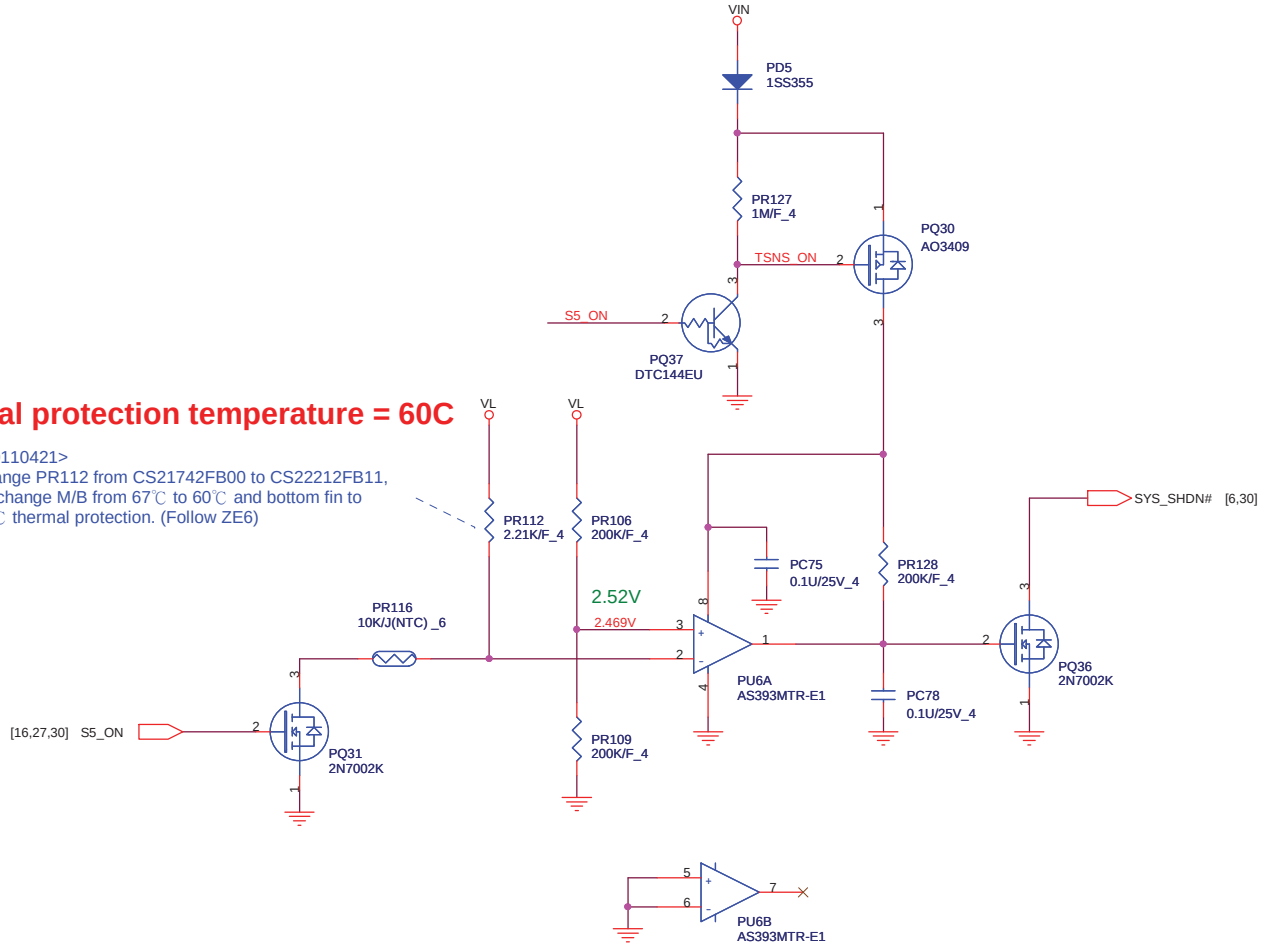
Thermal Protection (DCD)

Thermal protection temperature = 60C

<20110421>
Change PR112 from CS21742FB00 to CS22212FB11, for change M/B from 67℃ to 60℃ and bottom fin to 88℃ thermal protection. (Follow ZE6)



Quanta Computer Inc.
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Size	Document Number	Rev
	Thermal protect	C3C
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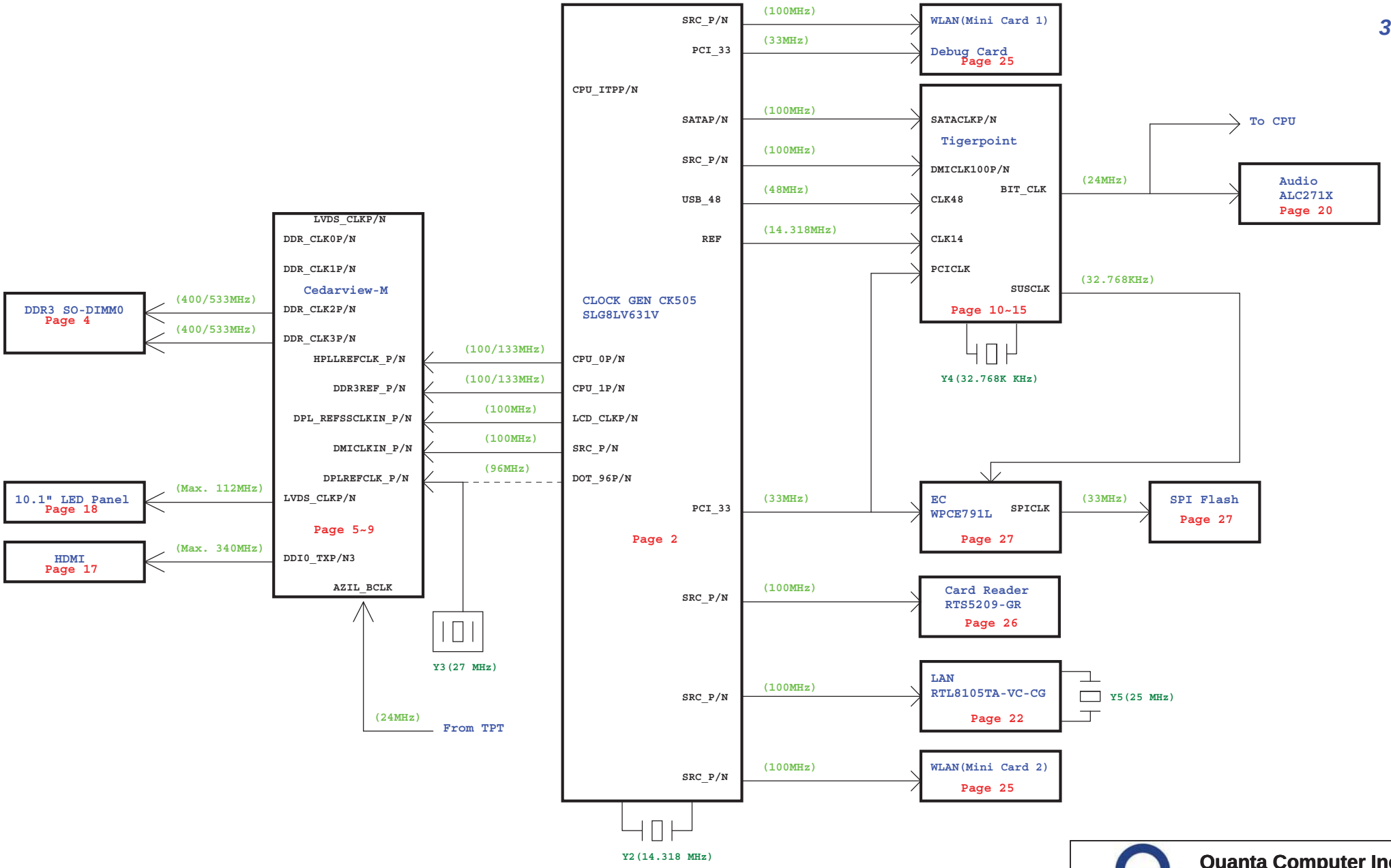

Quanta Computer Inc.

PROJECT : ZE7

Size	Document Number	Rev
	Clock Distribution Diagram	C3C
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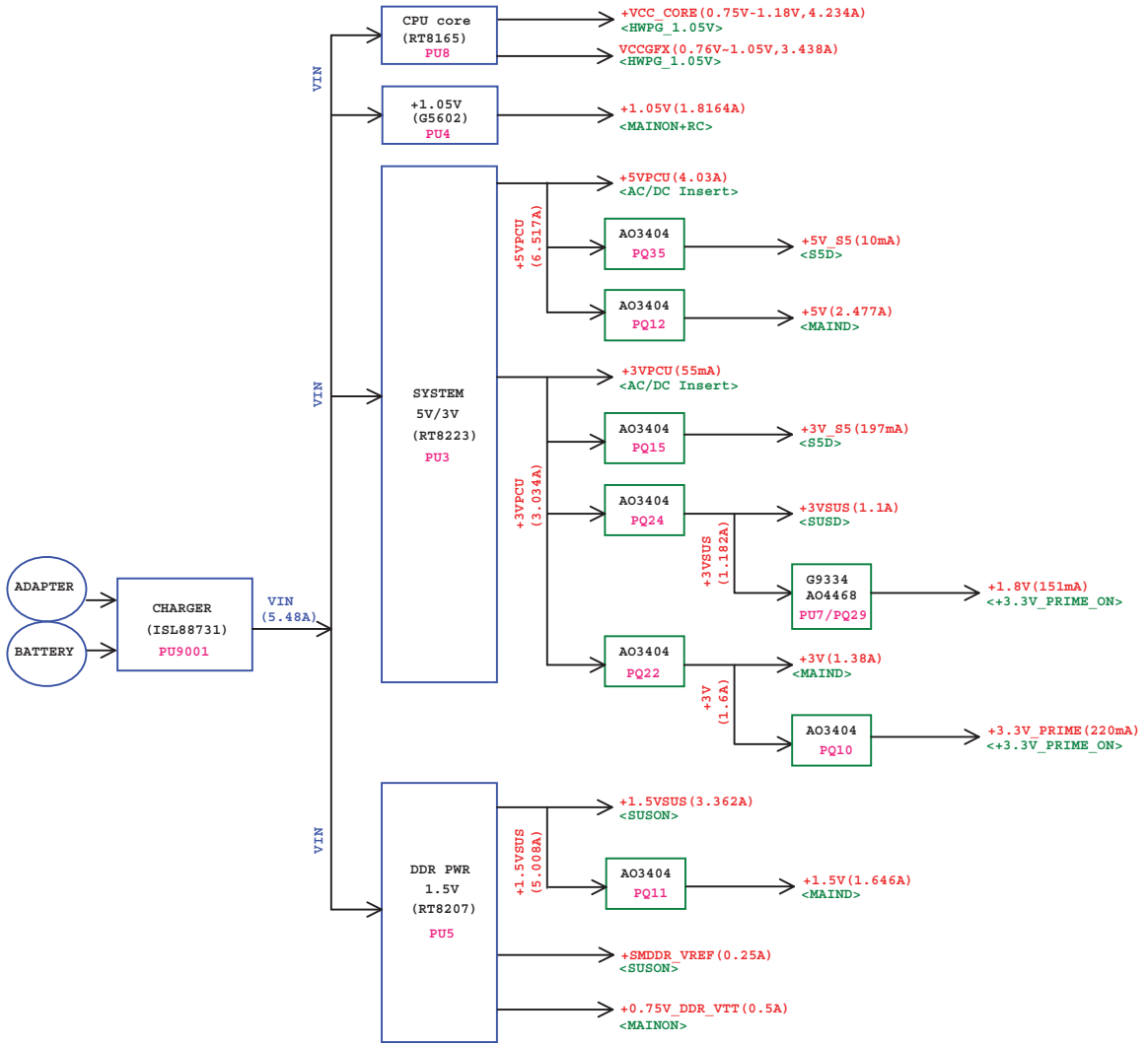

BOM Structure

	Function	Description	
3G	3G@	w/ 3G module	stuff 3G@
		w/o 3G module	unstuff 3G@
BT	BT@	w/ BT module	stuff BT@
		w/o BT module	unstuff BT@
LVDS/EDP	LVDS@	w/ LVDS (default)	stuff LVDS@ L38: CV+1003JN01 (0.1UH) C334: CH5102K9B06 (1UF)
	EDP@	w/ EDP	stuff EDP@ L38: CS00003J951 (0ohm) C334:CS00002JB38 (0ohm)
Deep Standby	DS3@	w/ deep standby (default)	stuff DS3@
	NS3@	w/ normal standby	stuff NS3@
PLL Power	1.5VPLL@	w/ 1.5VPLL (default)	stuff 1.5VPLL@
	1.05VPLL@	w/ 1.05VPLL	stuff 1.05VPLL@

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Power Tree
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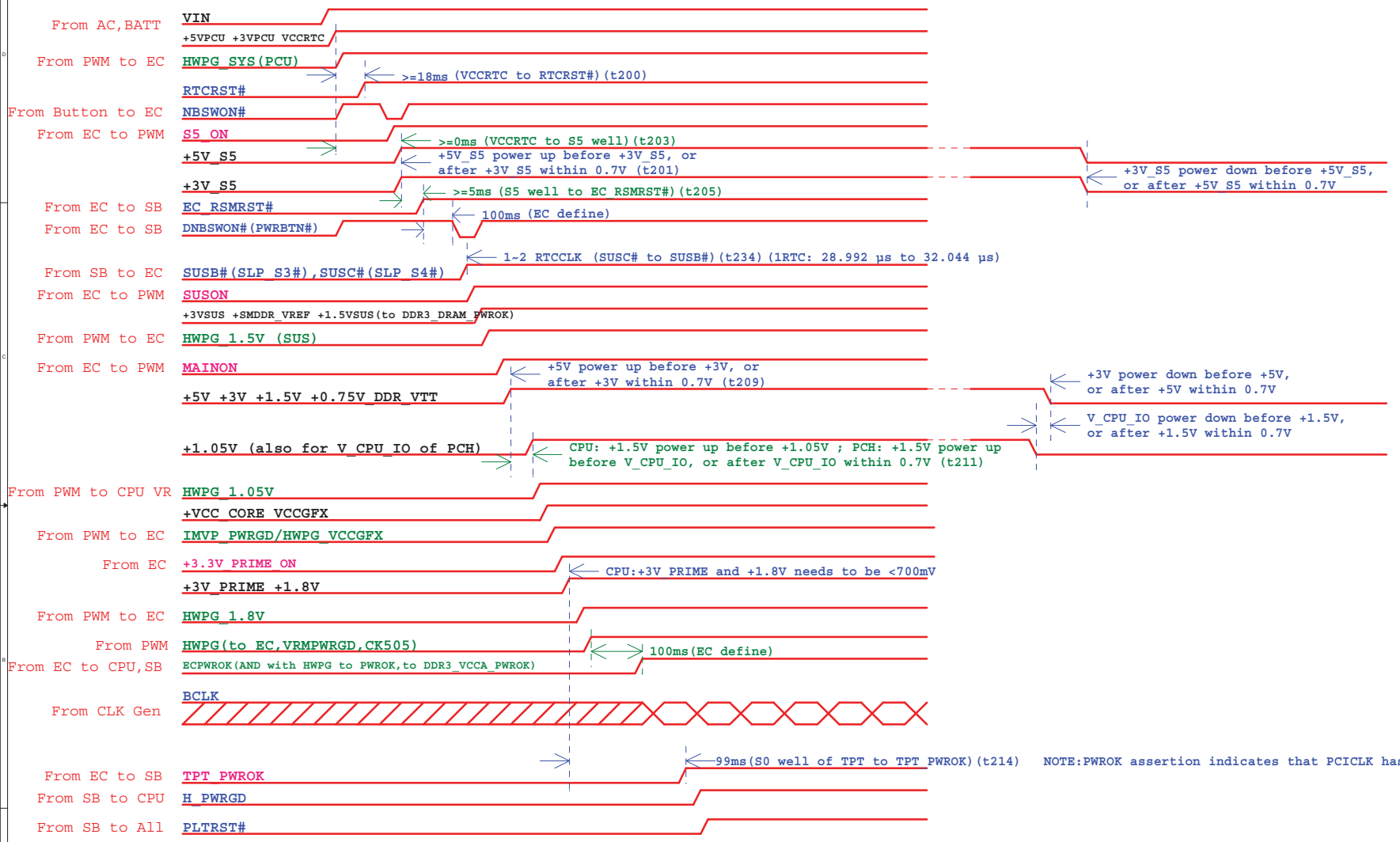
JE01_CT(Cedar Trail) Power On Sequence



*Note: EC will sampling SUSB# & SUSC# every 5ms.

ICH SMBUS Table

	CLK GEN	RAM	*Mini Card (WLAN)	*XDP	
(SMB_DATA)/(SMB_CLK) (+3V_S5)	V	V	V	V	
Power Plane	+3V	+3V	+3V	+3V	
MOS CKT (Level shift)	Stuff	Stuff	Stuff	Stuff	

*=Reserve

EC SMBUS Table

	Battery	CPU Thermal Sensor	GFX Thermal Sensor
EC791 SDA1 / SCL1 (+3VPCU)	V		
EC791 SDA2 / SCL2			
EC791 SDA3 / SCL3			
Power Plane	+3VPCU		
MOS CKT (Level shift)	X		

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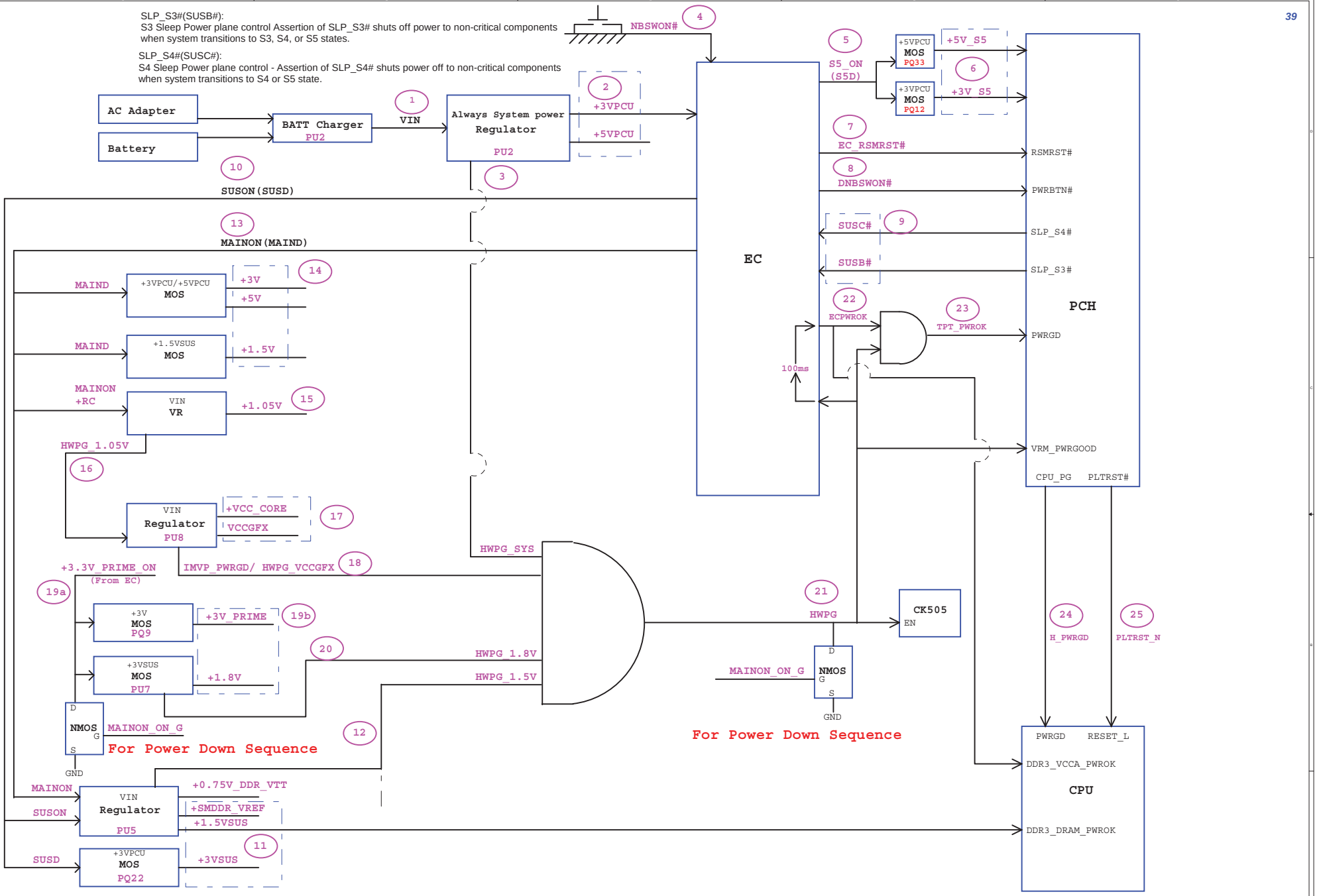
SLP_S3#(SUSB#):
S3 Sleep Power plane control Assertion of SLP_S3# shuts off power to non-critical components when system transitions to S3, S4, or S5 states.

SLP_S4#(SUSC#):
S4 Sleep Power plane control - Assertion of SLP_S4# shuts power off to non-critical components when system transitions to S4 or S5 state.



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power sequence block diagram
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Model	REV	CHANGE LIST	MODEL	ZE7 FROM	ZE7 To
ZE7 MB	D1A	20101124: <Page 27> Del net USB_EN#_1 / USB_EN#_2 / USBOC#R2 / USBOC#R1 / 5VUSB_3		C1A	D1A
		<Page 27> Add USB_EN# / USBOC#R		D1A	E1A
		<Page 10> Del USBOC0#/ USBOC3#/ USBOC1# ; Add USBOC#R_1/ USBOC#L_1			
		<Page 26> Add net SD_D2_R			
		20101125: <Page 26> Del net MS_CLK_R / PCIE_CLK_REQ1#			
		<Page 26> Delete R628; Reserve C510 for EMI (follow vendor CRB)			
		20101126: <Page 5> Add net name TX1_HDMI+ / TX1_HDMI- / TX2_HDMI+ / TX2_HDMI- / TX3_HDMI+ / TX3_HDMI-			
		<Page 5> Add net name TXLOUT0_R+_EDPTX1+ / TXLOUT0_R-_EDPTX1- / TXLCLKOUT+_R_EDPTX2+ / TXLCLKOUT-_R_EDPTX2-			
		<Page 5> Add net name LCD_CLK_R_EDPTX3+ / LCD_DATA_R_EDPTX3-			
		20101129: <Page 27> Change U14 from AKE38FP0N01 to AKE38ZP0N02 for EC request			
		<Page 20> Modify Headphone Jack schematic to follow ZE6			
		<Page 24> Add LED5 for power indicator			
		20101130: <Page 16> Delete SIO board connector			
		<Page 5> Stuff C432 to follow checklist0.7			
		<Page 7> Stuff C422; Unstuff C210/C111; Change C408 to 22U/6.3V_8/ C409 to 1U/6.3V_4 to follow checklist0.7			
		20101206: <Page 26> Change card reader connector P/N footprint due to ME request			
		<Page 29> Update battery connector to follow ZE6			
		20101209: <Page 17> Change HDMI connector to DFHS19FR015 by PDC suggestion			
		20101213: <Page 31> Delete PC120 at +VCC_CORE (Power team Duncan will use A3 M/B to verify again)			
		<Page 18> Reserve L21/ L22 /L40 /L41/ R253/ R255/ R258/ R259/ R262/ R263/ R265/ R269 for LVDS signals (RF suggestion)			
		20101216: <Page31> Reserve PC53/PC120 for EMI suggestion			
		<Page12> Reserve R356/ C290 for EMI suggestion			
		20101217: <Page20> Change CN10(internal speaker CONN) from DFHD04MR981 to DFHD04MRA75 (follow ZE6)			
		<Page28> Add NUT part number (follow ZE6)			
		20101220: <Page5> Swap DDI0_TX2_DP /DDI0_TX0_DP ; Swap DDI0_TX2_DN /DDI0_TX0_DN to correct HDMI channel			
		<Page22> Change RJ45 connector to DFTJ12FR221 to follow ZE6			
		20101221: <Page13> Change RTC battery from pin type to holder(DFHS02FS561)			
		20101228: <Page29-35> Update power budget description			
		<Page1-40> Update test pad size to TP2650			
		<Page29> Update battery connector P/N to DFAD08MR013 (follow ZE6)			
		20101229: <Page24> Unstuff HDD LED related circuit for cost down requirement			
		<Page31> Change PR71 to 5.72K_F cause VCCGFX power-budget has changed to 2.58A (Power budget V0.3)			
		<Page20> Modify speaker connector pin definition to follow PDC design			
		20101231: <Page20> Modify earphone and mic connector pin definition			
		20110103: <Page22> Modify CLKREQ_LAN#_R to CLKREQ_LAN#_R1 because netname duplicate			
		20110104: <Page13> Change EC_SMI# to GPIO10; Delete net PCH_GPIO10; Add net PCH_GPIO8			
		<Page20> Modify speaker connector pin definition back to original design			
		<Page19> Modify TP connector pin define to correct TP doesn't work issue			
		--Gerber out for A4-test--			
	E1A	20110105: <Page 25> Add net WLAN_LED1#			
		20110106: <Page 7> Change L8/ L12/ L13 from CV01001MN16 to CV01001MN08 for shortage issue			
		20110107: <Page 5> Add NCT7717U thermal sensor circuit (Reserve)			
		20110110: <Page 2> Add R515/ R516 for USB_48M CFG input hardware strapping to allocate PLL assignment. (Reserve)			
		<Page 10> Exchange USB port1 with port3 for S3 auto resume issue			
		20110111: <Page 21> Add USBP3-_L1/ USBP3+_L1/ USBP3-_L2/ USBP3+_L2/ USBP3-_L/ USBP3+_L/ CHARGE_IC_ON for USB charger reserve			
		<Page 20> Add net AMIC2_INT; Delete net LIN2_INT_R/ LIN2_INT_L for A-MIC (follow ZE6)			
		20110113: <Page 27> Add DNBSWON#_1 and D41 to solve +3V_S5 current leakage			
		20110117: <Page 20> Reverse CN4 connector routing for A-MIC cable design (follow ZE6)			
		20110119: <Page 2> Change R515 from 10K ohm to 20K ohm for vendor's suggestion. (Reserve)			
		20110124: <Page 25> Change net name from CLKREQ_MMC# to CLKREQ_3G#			
		<Page 25> Change R257 from 10K to 100K to solve leakage (follow ZE6)			
		20110127: <Page 18> Delete netname VCC_DDC			
		20110214: <Page 19> Change CP1-CP6 footprint from 8p4r-0402-smt to 8P4R for SMT open issue			
		20110221: <Page 2> Reserve 0.1F cap to solve that PCICLK (EC 33MHz) sometimes will change to 25MHz after flash BIOS and restart in first time issue.			
		<Page 2> Exchange PCLK_DEBUG and LCLK_EC for PCICLK issue.			
		20110224: <Page 18> Change C300 from 2.2U to 10U to solve LCDVCC fall time issue.			
		<Page 18> Add net +5V_LCD for IVO panel using			
		<Page 20> Reserve DMIC signals to co-layout with DMIC connector, reserve R526/ R527 add net AMICINT_DMICDAT / AMICGND_DMICCLK			
		<Page 10> Unstuff C111/ C123/ C125/ C133/ R78/ R79/ R84/ R86 to change DMI from x4 to x2			
		20110301: <Page 07> Change C326 from 10U to 47U; Add C386 47U for CRT flickr issue.			
		<Page 18> Change L15/ L16/ L17 from 47ohm to 22ohm; Remove C109/ C110/ C114 for CRT issue			
		<Page 18> Change C79/ C80/ C81 from 22pF to 4.7pF for CRT issue.			
		20110302: <Page 35> Reserve PR129 for no use			
		20110303: <Page 5> Reserve DDI1 PU resistors R529 to follow CRB(eDP); Add net DDI1_DDC_SCL/ DDI1_DDC_SDA			
		<Page 20> Reserve L42/ L43/ L44/ L45 for ESD solution			
		20110304: <Page 20> Change R525 from 0603 short pad to 0603 0ohm			
		<Page 25> Unstuff PD8/ PR106/ PR133 for no use			
		<Page 5> Stuff R512/ R513/ U26/ C381/ C382/ R514/ R509/ C384/ C383 for thermal sensor			
		<Page 27> Stuff R175/ R160 for thermal sensor			
		<Page 24> Unstuff C320 for cost down			
		20110307: <Page 18> Reserve R530 for eDP function hardware short term solution			
		20110308: <Page 23> Reserve stitching cap for RF suggestion			
		<Page 24> Unstuff C320 for cost down			
		<Page 35> Delete PR106/ PR113/ PD8/ PR129 (thermal protection) for unused circuit (follow ZYG)			
		<Page 28> Change Hole16/ Hole17 footprint to h-tc177bc295d120p2			
		<Page 5> Delete R510/ R511 for thermal sensor SMBUS PU (PU at EC side)			
		<Page 5> Unstuff C384/ C383; Change C382 from 10U_8 to 4.7U_6			
		<Page 6> Reserve R531 for thermal sensor test			

DOC NO.	PROJECT MODEL :	ZE7	APPROVED BY:		DATE:	
	PART NUMBER:		DRAWING BY:		REVISON:	

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Model	REV	CHANGE LIST
ZE7 MB	E1A	20110308: <Page 13> Unstuff R451 for using thermal sensor (Need stuff when no use thermal sensor) <Page 27> Change thermal sensor SMBUS PU from +3V_S5 to +3V <Page 28> Change Hole18/ Hole19/ Hole20 footprint to h-c197d63p2 <Page 18> Add R510 for eDP function verifying
		20110309: <Page 28> Add hole23 <Page 20> Change R525 from 0603 short pad to 0402 0ohm --Gerber out for A5-test--
	F1A	20110309: <Page 20> Change R525 from 0603 short pad to 0402 0ohm
		20110314: <Page 27> Change U7(BIOS) to AKE38FP0Z01 (follow ZE6)
		20110315: <Page 20> Change L27 from CS00004JA40 to CX121T30001 <Page 20> Delete R208/ R261/ R433/ R475 for CS00003J951
		20110318: <Page 29> Change DC jack to DFPJ03MR043 (follow ZE6)
		20110328: <Page 28> Change Thermal nut to MBZH5002012 (follow ZE6)
		20110330: <Page 2> Change R236 PU connect from PM_STPCPU# to PM_STPCPU#_R
		20110406: <Page 24> Change R329 from CS11202JB21(120ohm) to CS05102JB35(51ohm) PWR light <Page 24> ChangeR326/ R323/ R321 from CS12702JB14(270ohm) to CS12002FB25(200ohm) Blue light <Page 24> ChangeR327/ R324/ R322 from CS14702JB28(470ohm) to CS13302FB11(330ohm) Amber light <Page 22> Unstuff R341/ R330 for W/O LED RJ45 CONN (follow ZE6) <Page 27> Del T44 for no use of CIR uart function, will place T34 for ICT programming
		20110407: <Page 28> Add GND PAD1 for LED ESD using <Page 16> Unstuff R100/ R142/ R143/ R132/ R96/ R97 for height limit
		20110412: Change Q1/ Q27/ Q34/ Q35/ Q39/ Q42/ Q43 from BA0390400H0 to BA039040020 for EOL issue Change PL1/ PL2/ PL6 from CX0R800R014 to CX12T800000 for EOL issue (EMI Sam provide) <Page 18> Change MR1 from AL003661003 to AL002618001 for EOL issue (ZE6 2nd source)
	G1A	20110413: <Page 30> Change PU3 from AL008206002 to AL008206000 <Page 23> Add C388/ C389 stitching caps for monitor flickr issue <Page 11> Add net CPUSLP# / CPUSLP#_R and add R511/ R532 to reserve CPUSLP function
		20110414: <Page 22> Change D35 from CY640P31Z08 to CY003100Z06 for cost down <Page 13> Stuff R451 to reserve thermal sensor function <Page 9> Unstuff C381/ C382/ R509/ R512/ R513/ R514/ U26 to reserve thermal sensor function <Page 27> Unstuff R175/ R160 to reserve thermal sensor function <Page4> Modify DDR DQ/ DQS/ DM signals to no swap type
		20110418: <Page29~35> Change Power solution for ZE7 project <Page 23> Delete C389 for CRT DAC stitching cap <Page 30> Change JP1007 footprint to RC3720-SMT
		20110420: <Page 11> Delete net CPUSLP# / CPUSLP#_R and delete R511/ R532 to remove CPUSLP function (nettop platforms only) <Page 20> Change R178/ R477 from 75ohm to 47ohm for earphone gain fine tune (follow ZE6)
		20110422: <Page 18> Change MR1 from AL002618001 to AL003661006(PT3661G-BB) for Lid switch issue <Page 30> Delete PC1032 for power request <Page 31> Delete PC1019; Add PR1104; Change PQ1001 (Dual MOS) to PQ1001 & PQ1008 (3X3 QFN) <Page 9> Un-stuff R149/ R151/ R478/ R479 to solve leakage issue <Page 18> Change C138 from 0.1U_6 to 4.7U_8 to solve hall sensor issue
		20110425: <Page 25> Change U7 from AKE38FP0Z01 to AKE38FP0N01 for ICT MAC ID issue <Page 18> Change C138/ C318 from 4.7u_8 to 4.7u_6 (CH5471K9E07)
		20110426: <Page 13> Add C389 0.1U_4 for TPT_PWROK glitch issue <Page 2> Change Y2 from BG614318242 to BG614318F33 for new part
		20110427: <Page 26> Change C267/ C268 from 22P/50V_4 to 10P/50V_4 for EMI request <Page 26> Add R511 and net MS_CLK_R for EMI request <Page 26> Change R271/ R285/ R290/ R299/ R305/ R313 from 0ohm to 33ohm for EMI request
		20110428: <Page 26> Del R511 and net MS_CLK_R, change R303 from 0ohm to 33ohm for EMI request <Page 13> Reserve C390 30P_4 for EMI request <Page 20> Add C391 1n_4 for amic noise depressing (Realtek Vic suggest) <Page 31> Add PC1019/PC1032 2200p_4 for EMI request <Page 30> Change PC1043/ PC1046 from 330uF to 220uF; Change PL4 from 3.3uH to 2.2uH <Page 30> Change PR1098 from 4.7K ohm to 48.7K ohm
		20110429: <Page 13> Stuff R85,R449,R455 for ZE7 A2 stage (Board ID PD) <Page 20> Change R178/ R477 from 47ohm to 56ohm to meet acer Full Scale Output Voltage (FSOV) spec <Page 13> Reserve R511 0ohm and RTCRST#_EC for RTC reset workaround solution <Page 19> Stuff CP1~CP6 for EMI Sam request
		20110506: Rename <Page 17> Unstuff R138 to follow CRB
		20110510: <Page 18> Change MR1 from AL003661006(PT3661G-BB) to AL009132001 (CMOS type) <Page 18> Change C138 from 4.7U_6 to 1U_6; Unstuff R91 because MR1 is CMOS type <Page 22> Change C4/C7 from 27P to 33P(CH03306JB04) by vendor fine tune result
	A3A	20110516: <Page 11> Add R532/ R533 and net CPUSLP#_R / CPUSLP# (enable C6-state) <Page 17> Add R534/ R535 PU 2K for HDMI I2C to follow CRB <Page 24> Del SW4 for no use <Page 5> Change C334/ C335 from 18P_6 to 33P_4 for crystal vendor's report <Page 18> Add R536/ D44 for MR1 EOS protection <Page 10> Modify USBOC pin <Page 13> Change CN5 to DFHS02FS032 for SMT issue <Page 13> Change R93/ R454/ R472/ R468 from CS03302JB29 to CS09092FB15 (RES CHIP 90.9 1/16W +-1%(0402)) to follow CRBv1.5 Remove Deeper Standby/ XDP/ DMIC/ USB charger function
		20110520: <Page 8> Change R99 from 12.1K to 121ohm to follow CRBv1.5 <Page 8> Change R98 from 10K to 100ohm to follow CRBv1.5
		20110525: <Page 30> Modify JP9 footprint to RC3720-SMT for SMT open issue
		20110530: <Page 24> Modify LED4 from +3V to +5V Due to there is the internal series resister in 3G/WLAN module, cause the forward voltage of LED4 is too small
		20110531: <Page 29~35> Update power portion
		20110601: <Page 26> Modify CN20 (Card reader CONN) footprint to 7in1-cm7r-052-h-d-44p-smt by SMT ME Peter request <Page 23> Change C140 from 0402 to 0603; Del C141 <Page 29> Change PU9001 to PU2; Change PU2 footprint from QFN28-5X5-5-33P to QFN28-5X5-5-33P-SMT <Page 31> Add Power Jumper for power consumption measurement

MODEL	ZE7 FROM	ZE7 To
	C1A	D1A
	D1A	E1A
	E1A	F1A
	F1A	G1A
	G1A	A3A

DOC NO.					
PROJECT MODEL :	ZE7	APPROVED BY:		DATE:	
PART NUMBER:		DRAWING BY:		REVISON:	

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Model	REV	CHANGE LIST	MODEL	ZE7 FROM	ZE7 To
ZE7 MB				C1A	D1A
				D1A	E1A
				E1A	F1A
				F1A	G1A
				G1A	A3A
				A3A	B3B
		20110602: <Page 7> Del R490 and short for VCCCKDDR_VSM			
		20110603: <Page 23> Del C215 for no use(DMIC stitching cap for RF)			
		20110607: <Page 2> Delete R287/ R288/ T28 /T29 since SIO board was canceled <Page 2> Delete R238/R239/ CLK_PCIE_MNC_XDP_N/ CLK_PCIE_MNC_XDP_P and short directly since XDP was canceled <Page 25> Un-stuff R314,R294 since all of WLAN modules don't use SMBUS <Page 21> Change USB_CHARGE_ON to USB_EN#, delete R524/ USB_BC_EN and short , change U25 to AL000547005 since charge IC was canceled <Page 31> Add PC123(100u/25V_6X5.8) to suppress VIN noise <Page 11> Stuff R105_1K for IGNNE to follow CRB design <Page 13> Del R396/ R387, stuff R407/ R382 for PCH_GPIO12/ PCH_GPIO13 (PU for no use) <Page 4> Unstuff C200 /C190 for +0.75V_DDR_VTT <Page 4> Unstuff C203 for +1.5VSUS <Page 7> Change R31/ R45/ R32 from 10uF_8 to 4.7uF_6 <Page 7> Change C362 from 22uF_8 to 10uF_8			
		20110608: <Page 27> Reserve D22. stuff R281 for +3V_EC; Change D22 from BC000316Z07 to BCRB500VZ29 <Page 31> Add PC123-PC127 to supress Vin noise <Page 27> Reserve D13/D14/ D17/D21 for HWPG			
		20110609: <Page 25> Un-stuff C9 since EM820W doesn't use Vpp <Page 13> Change Y4 from BG332768A01(20PPM/12.5PF) to BG332768542(20PPM/7PF), and change C348,C349 from 15pF_4 to 6pF_4 Change D8,D10,D19,D23,D24,D25,D39,D41 from BC000316Z07 to BCRB500VZ29			
		20110610: <Page 24> Change R330/ R327/ R325 to 51ohm_4 for Blue LED; Change R331 to 220ohm_4; Change R328 to 270ohm_4 for Orange LED --Gerber out for C-test--			
	B3B	20110614: <Page 6> Stuff R33 PU 1k ohm(CS21002JB34) to +3V for DBR# by Intel Nick confirming <Page 31> Change PR138 from CS41602FB00 to CS42742FB00 by Duncan request			
		20110622: <Page 24> Change R330 from CS05102JB35(51ohm) to CS03302JB29(33ohm) to meet LED brightness spec. <Page 24> Change R327 from CS05102JB35(51ohm) to CS03302JB29(33ohm) to meet LED brightness spec. <Page 24> Add R328 for CS12202FB14(220ohm) to meet LED brightness spec. <Page 24> Change R325 from CS05102JB35(51ohm) to CS11502FB21(150ohm) to meet LED brightness spec. <Page 24> Change R326 from CS13302FB11(330ohm) to CS14702JB28(470ohm) to meet LED brightness spec.			
		20110627: Change 0ohm resistors to short PAD			
		20110628: Remove common choke footprint Remove power short jumper <Page 2> Unstuff R229 CS00002JB38 for CPU_STOP# to follow checklist rev1.5 <Page 5> Remove R411 / R412 CS00002JB38 and short for CRT_HSYNC / CRT_VSYNC <Page 13> Stuff R513 CS00002JB38 (0/J_4) for RTCRST#_EC ; Stuff R417 for PLT_RST# <Page 18> Stuff R26 CS00003J951 (0/J_6) for +5V_LCD (IVO panel) <Page 20> Stuff R203/R444 CS00003J951 (0/J_6) for audio ESD solution			
		20110630: <Page 20> Change CN15/CN13(Audio Jack CONN) footprint from phjk-2sj2326-002111-6p to phjk-2sj2326-002111-6p-smt for SMT open issue Change PR65/PR66/PR39/PR29/PR153/PR22/PR36/PR152/PR160/PR161 footprint from RC0402 to short0402 by power Duncan request <Page 31> Stuff PC7 CH14706KB18 (470p_4) for GFX issue <Page 10> Un-stuff C346/ C347 for no support PCI-E in 3G card <Page 18> Remove C324 for LCDVCC power <Page 20> Change C230,C221,C234,C247,C263,C265 from CH6101M9905 (10uF_6) to CH5471M9907 (4.7uF_6) for Audio power <Page 5> Un-stuff R62 to reserve eDP function Unstuff C69; Change C20/C137/C157/C298/C310/C309/C387 from (10uF_8) to CH5472K9A02 (4.7uF_8) <Page 5> Change R38/R39 from 4.7K to 2.2K for EDID(follow CRB). <Page 29> Unstuff PU1 (battery connector ESD solution)			
	Ramp	20110705: <Page 25> Swap USBP7+/USBP7- to correct Wimax function. <Page 20> Stuff BC040201Z00(TVS/6pF_4) at D9 for analog mic ESD solution			
		20110707: <Page 8> Stuff CS41002JB20(100K_4) at R474 for DDR3_DRAMRST#_R by Intel Nick confirming by Richtek's feedback			
		20110708: <Page 31> Change PC7 from CH14706KB18(470p/50V_4) to CH13306JB14(330p/50V_4) for GFX compensation.			
		20110711: <Page 18> Change R536 from CS00003J951(0_6) to CS04703F912(47_6) to increase hall IC ESD protection level			
		20110719: <Page 20> Change R172/R497 from CS05602JB17(56_4) to CS04702FB16(47_4) for FAE Vic suggestion to meet acer FSOV spec			
		20110721: <Page 21> Change U23/U25 footprint from MSOP8-4_9-65-9p to MSOP8-4_9-65 to cancel GND pad for SMT open issue			
		20110725: <Page 8> Add CH4103K1B08(0.1U/16V_4) cap footprint at C159 for Elpida DDR 2A issue debugging (to suppress glitch)			
		20110727: <Page 8> Reserve 1U/10V_6 cap footprint at C388 for DDRAM_PWROK RC delay <Page 32> Un-stuff PR121 CS41002FB28(100K/F_4) PU for DDRAM_PWROK because D14 is un-stuff at EC side <Page 32> Add PR198 0/J_4 for DDRAM_PWROK <Page 32> Del netname HWPG_1.5V and change to DDRAM_PWROK			
		20110804: <Page 20> Change L25 from CX121T30001 (120ohm bead) to CS00004JA40 (0_8) by EMI confirmed <Page19> Un-stuff CA122084N98 at CP1 - CP6 by EMI confirmed <Page26> Reserve C282/C284/C291/C296/C392/C393 CH01006JB08 (10p_4) by EMI confirmed			
		20110805: <Page 20> Reserve R520 0_6 footprint for analog mic ESD protection <Page 20> Stuff R501 0_6 for analog mic ESD protection			
		20110811: Change PC7 from 330p_4 (CH13306JB14) to 100p_4 (CH11006JB00) for power GFX issue			
		20110819: <Page 18> Change R75/R76 from CS01802JB13(18/J_4) to CS04702FB16(47/F_4) <Page 18> Change L16/L17 from CX8BA220007(0.5A/22ohm_6) to CS00003J951(0/J_6)			
		20110830: <Page 8> Change R537/R539 from CS00002JB38(0_4) resistors back to 0402 short pad for Elpida DDR 2A issue debugging			
		20110831: <Page 26> Connect CN20(Card reader CONN) pin27 to GND by EMI Sam suggestion <Page 20> Add R520 CS00003J951(0_6) for analog mic ESD protection <Page 28> Modify Hole1 footprint from hg-c276do94x106p2 to ZE7-P3 for power button ESD solution <Page 28> Modify Hole15 footprint from HG-C276D98P2 to ZE7-P1 for touch pad ESD solution <Page 28> Modify Hole16 footprint from HG-C276D98P2 to ZE7-P2 for touch pad ESD solution <Page 28> Add GND PAD2 for touch pad ESD solution			

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